Shaded areas of data tables indicate data that is to be taken in the lab. All other data should be completed prior to attendance in the lab session. The instructor will sign the data sheet to indicate that required preliminary lab work has been completed.

Introduction: This experiment will demonstrate the properties and illustrate some of the applications of digital multiplexers and demultiplexers through the design, implementation and exercise of example circuits. These devices are the digital equivalent of rotary switches that have the ability to select one of several sources for a single destination (multiplexer) or distribute one source out to several destinations (demultiplexer.) These circuits can be configured in a variety of ways to perform a variety of functions. This experiment will demonstrate their use in creating sum of products functional expressions and their use in parallel-to-serial conversions.

The Digital Multiplexer as a Sum-of-Products Function Generator.

The digital multiplexer can be used to provide both the minterm generation and the summation needed to implement SOP expressions. Consider the following sum-of-products expression:

\[ Y = f(A, B, C) = \overline{A}BC + \overline{A}BC + \overline{A}B + \overline{B}C \]

\[ \text{Expression 2.1: Conventional SOP Expression} \]

To implement this expression with a multiplexer, it must first be expanded into each of its unique minterms. It is advantageous to express the final argument in summation form:

\[ Y = f(A, B, C) = \overline{A}BC + \overline{A}BC + \overline{A}B + \overline{B}C \]

To implement this expression with a multiplexer, it must first be expanded into each of its unique minterms. It is advantageous to express the final argument in summation form:

\[ Y = f(A, B, C) = \overline{A}BC + \overline{A}BC + \overline{A}B + \overline{B}C \]

This configuration is shown in Figure 2.1 implements the summation expression. Note that the inputs to the multiplexer that are identified as TRUE (logic 1) in the summation expression are tied to a logic 1. The remaining inputs are tied to a logic 0. When used in this configuration, the multiplexer will act as a “rotary switch,” to provide the value on the addressed D input on the Q output. Therefore, if \( \overline{A}BC = 000 \), the input on D0 will be present on the output of the multiplexer. According to our expression, minterm 0 is to be TRUE, and it has been tied to a logic 1.

Instructor’s signature indicating that pre-lab work has been completed:
Part One, steps 1-3. Part Two steps 1-3, Part Three step 1.
Design, construct, and test a circuit which uses an SN74151 to implement a sum-of-products expression.

**Step 1.** Convert expression 2.3 to summation form:

\[ Y = f(A, B, C) = A\overline{B} + \overline{B}C \]

**Expression 2.3**

**Step 2.** Sketch on (Figure 2.2) the input connections necessary to implement the function of Expression 2.3.

**Step 3.** Fill in the column labeled Y of Table 2.1 with the anticipated output logic of the 8-to-1 multiplexer configured to generate the function of Expression 2.3.

**Step 4. To be completed in lab:** Figure 2.4 illustrates the pin diagram and logic specifications of the SN74151 data selector/multiplexer.

1. Place an SN74151 chip on a breadboard and assemble the connections to implement the completed circuit illustrated in Figure 2.2.
2. Apply power to the circuit.
3. Stimulate inputs A, B, and C, to complete the Y’ column of Table 1.1. The two columns, Y and Y’, should be the same.
4. Demonstrate the circuit to the instructor and obtain a signature below, indicating proper operation:

```
<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A B C</td>
<td>Y Y’</td>
</tr>
<tr>
<td>L L L</td>
<td>L H</td>
</tr>
<tr>
<td>L L H</td>
<td>L H</td>
</tr>
<tr>
<td>L H L</td>
<td>L H</td>
</tr>
<tr>
<td>L H H</td>
<td>L H</td>
</tr>
<tr>
<td>H L L</td>
<td>L H</td>
</tr>
<tr>
<td>H L H</td>
<td>L H</td>
</tr>
<tr>
<td>H H L</td>
<td>L H</td>
</tr>
<tr>
<td>H H H</td>
<td>L H</td>
</tr>
</tbody>
</table>
```

**Table 2.1**

![Figure 2.4a: SN74151 Truth Table](image)

![Figure 2.4b: SN74151 Pin Configuration](image)
PART-TWO: Design, construct, and test a circuit which uses an SN74138 demultiplexer to implement a sum-of-products expression.

**Step 1.** Convert expression 2.4 to summation form:

\[ Y = f(A, B, C) = \overline{ABC} + \overline{BC} \]

*Expression 2.4*

**Step 2.** The demultiplexer output is selected, and will go low, by the address on inputs A, B, and C when the IC is enabled. Therefore, we can create the output function Y by summing together the outputs indicated by the summation form of Expression 2.3. Since the outputs of the demultiplexer are active-low, this is done with a NAND gate. Connect each of the TRUE minterm outputs of the demultiplexer in Figure 2.5 (indicated by the summation equation) to an input of the NAND gate. Connect all unused NAND inputs to a logic 1.

**Figure 2.5**

**Step 3.** Fill in the column labeled Y of Table 2.2 with the anticipated output logic of the 3-to-8 demultiplexer/NAND circuit configured to generate the function of Expression 2.4.

**Step 4.** To be completed in lab: Figure 2.6 illustrates the pin diagram and logic specifications of the SN74138 data selector/multiplexer.

5. Place an SN74138/SN7420 chip pair on a breadboard and assemble the connections to implement the completed circuit illustrated in Figure 2.5.

6. Apply power to the circuit.

7. Stimulate inputs A, B, and C, to complete the Y' column of Table 2.2. The two columns, Y and Y', should be the same.

8. Demonstrate the circuit to the instructor and obtain a signature below, indicating proper operation:

**Table 2.2**
PART-THREE: Design, construct, and test a circuit using an SN74151 that will convert 8 bits of parallel data to a serial stream of data on the output. Use an LED to signal a logic 1 output on the output line.

Step 1. Connect any data (logic 1’s or 0’s) to the inputs of the SN74151. You must simulate a counter circuit on the A, B, and C inputs to select each bit of data to be placed on the output line.

Step 2. To be completed in lab:
1. Build the circuit of Figure 1.7
2. Apply power to the circuit.
3. Stimulate inputs A, B, and C, and data inputs D0 through D7 to demonstrate circuit operation.
4. Demonstrate the circuit to the instructor and obtain a signature below, indicating proper operation:

NOTES:

Parts List:

(1) Logic Trainer
(1) SN74151 8 to 1 Multiplexer/Data Selector
(1) SN74138 3 to 8 Demultiplexer
(2) SN7420 4-Input NAND Gate