Designing for Testability

Follow as many of these specifications as possible as a guide to designing a circuit board that is the most cost effective and efficient to test. Not meeting all these specifications does not mean the board is untestable. It just means it may be a little more expensive to build the test fixture.

What is Testability?
Testability can best be described as the ease with which the functionality of any electronic product circuit or component can be determined to a desired degree of accuracy. To put it more simply, how easily can it be checked for performance to-spec throughout the entire product life cycle from product concept through design, manufacture, and service? How quickly can test programs be generated? How accessible are the test points? How comprehensive is the fault coverage?

Testability is not a technological innovation. It is a mindset that creates a constant awareness of the importance of ease-of-testing ... in engineering ... during production ... in the field. Testability is critical to the manufacturing process -- *a product that cannot be readily tested is not really manufacturable.*

Non-testability costs; testability pays.
Unpredictable production schedules, bonepiles of suspect boards, a very high cost of test, and an uncertain level of product quality delivered to the customer... these are the indirect costs of non-testability. Add the time spent trying to diagnose, and you quickly see that non-testability can be very expensive.

Testability, on the other hand, is introduced at the design stage, where it dramatically lowers the cost of test and the time spent at test. Properly managed, testability heightens your assurance of product quality and smoothes production scheduling.

The State of Combinational Test Technology.
There are basically two approaches to test -- functional and in-circuit test

Functional Test -- Verifying the Entire Board.
Functional test is characterized by powering up the board and the application of input stimuli and measurement of the output signals on the circuit board. The measured output is compared against an expected result.

Functional test is aimed at verifying the functionality of the entire board. Functional test systems can be executed effectively at the speed of the design.

Functional test systems offer the potential of very high fault coverage and high confidence in the test results. However, functional test is based on two assumptions: the degree to which simulation technology can be applied to generating the test program, and the degree to which diagnostic strategies can be developed in a cost-effective and timely manner.

In-Circuit Test -- Verifying the Components and the Assembly Process.
In-circuit test is characterized by not powering up the board, but applying stimuli and measurement of the signal nodes on the circuit board. In-circuit test is best described as testing the functionality of each component on the board, with the inference that the overall board functionality can be verified by the fact that each component functions and that it is wired properly.

In-circuit test generally does not execute at the speeds of the design, due to the fact that the physics of back-driving limits the technique's practicality to a range of between I and 10 MHz test speeds. Test access is assumed to be available at each node to support the effectiveness of this testing philosophy.

Combinational Test
In-circuit test has essentially moved in two different directions, namely:

1. The Manufacturing Defect Analyzer (MDA) is a highly simplified in-circuit tester that uses analog measurements to verify the manufacturing process. Primarily used on fairly simple circuit boards, the MDA is a low-priced test alternative that can provide good fault coverage for simple analog components and circuit interconnection. It provides no fault coverage for component functionality on digital, complex analog or mixed signal devices.
2. The Combinational Tester is currently the most popular method of board testing. This system combines the capability of an in-circuit tester with that of a functional test system to achieve very high fault coverage and excellent diagnostic accuracies. In addition to the high component coverage afforded by in-circuit analog and digital test techniques, the combinational tester supports analog, mixed-signal, and digital functional testing. It also supports the newer test and diagnostic concepts such as Boundary Scan, NAND Trees, and digital opens detection using analog means.

Combinational Testability.
In order to design-for-testability, it is necessary to have a basic understanding of the capability of the combinational tester to provide test and diagnostics. This is best accomplished by examining the hardware, software, and fixturing technologies that support combinational test

Automatic Test Generation (ATG) has greatly enhanced the acceptance of combinational testing technology as a viable, cost-effective test approach. The ATG paradigm requires that information be available describing the components on the board (test models), their interconnects (circuit description), and their physical location (assembly).

Automatically capturing design information into the test generation process speeds test program development. The lack of the design data, on the other hand, can severely limit test effectiveness.

ATG algorithms calculate the effect of the circuit on the ability to stimulate and to measure the attributes of each component In addition, ATG algorithms have to recognize the measurement accuracies and timing capabilities of the combinational tester hardware.

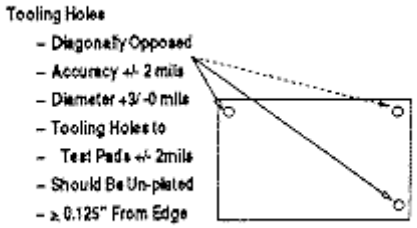
The capability of the tester to effectively isolate each component to accomplish the highest fault coverage test requires that analog "guard" and digital "inhibits and disables" be automatically entered into the program in order to minimize test development time.

The principal limitation to automatic test generation involves the lack of design data to create a test model for the devices on the board and to develop accurate fault coverage.

Circuit Board Design Files.
If possible, have your designer create a layer in the circuit board design files for test points and tooling pins. This will allow the creation of a Gerber file specifically for the test pads and tooling pins. Example: file name of test.gbr. Although this is not necessary, it helps speed fixture design and reduce costs and the potential for fixture fabrication error.

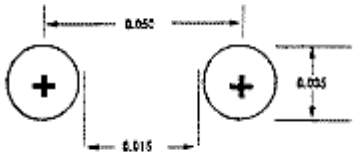
Mechanical Design Considerations.
PCB test access is typically accomplished through a bed-of-nails fixture, or higher performance short-wire fixtures. On automated manufacturing production lines where boards arrive at the ATE via conveyors, mechanically actuated fixtures are used.

Edge Clearances
Mechanical board handlers may need as much as 0.138" clearance from components and 0.125" clearance from test pads to provide room for conveyor rails.



Tooling holes

Tooling Holes
Place two (or three) diagonally opposed, unplated tooling holes as far apart as possible with a tolerance between holes of ±0.002" to ensure correct fixture placement. Tooling pin flex can be minimized by using at least 0.125" diameter holes. Tooling hole diameters should be maintained to within 0.003"/-0.000". Solder contamination and plating thickness variation problems can be prevented by keeping tooling holes free of plating.



Minimum Optimal Test Pad Positioning and Size

Test Pads
The tolerance from a test pad to tooling hole should be held to ±0.002". Clear access to test pads is vital. Ideally, test pads should be provided on each node. If possible, always place test pads on one side of the board to minimize the likelihood of more expensive double-sided fixtures. Test pads should be round, and nominally 0.035" in diameter with pad-to-pad accuracy of ±0.003".

Board Edge
Test pads should also be located at least 0.125" from the board edge because, pick and place systems and handlers require access to the board edges.

Spacing
Test pad spacing should be 0.100"whenever possible, 0.050" at a minimum. Test Electronics can probe centers as close as 0.015", but these small probes are expensive and do not have the durability of the larger probes.

Component Clearance
Test pads on the component side of the board should have at least 0.040' clearance from components to avoid damage to either the probe or the part.

Proximity to Signal Source
Place test points as close as possible to the signal source to minimize the electrical impact of the tester on the circuit board. Place several test pads on the VCC and ground lines to assure a more even power distribution. Keep in mind that heavy backdrive currents can shift ground potentials.

Accessibility Guidelines for SMT Boards

Test pads should be 0.015 to 0.040 inches in diameter.
Based on generally accepted test fixture/PCB manufacturing tolerances, the SMD probe requires a test pad of this size for repeated tip-to-target accuracy. Naturally, the larger the target, the greater probability of hitting it
Coat test pads with conductive non-oxidizing material.
Test pads should be solder-coated or coated with a non-oxidizing material such as gold. Solder oxides are easily penetrated with most sharp tip styles, ensuring good electrical integrity.
Probe test pads or vias, not components or component leads.
Probing a component lead may force a broken or cold solder joint to make contact and appear good.
Provide accurate tooling pins.
The tooling pin location is key to fixture/PCB alignment Tolerance from the DUT to the datum to the test pad should be ±0.002 in.
Place tooling holes as far apart as possible.
Tooling holes on the PCB should be as far apart as possible, diagonally placed, with a tolerance between holes of ±0.002 in. A 0.125 in. or larger tooling pin will help maintain stability and PCB/fixture alignment.
Tooling hole diameter tolerance should be within +0.003/ -0.000 in.
Minimize use of tall components.
SMT boards with component height greater than 0.35 in. are difficult to probe, requiring cutouts or relief in the probe plate. When possible, extend test pads 0.1 in. away from tall components to allow for milling tolerances.
Don't crowd test pads.
Leave a 0.018 in. unpopulated area around each test pad to minimize shorting during worst-case tolerance scenarios.

Probing
Device pins (through-hole), test pads, connectors, and vias can be used to allow adequate test access. For PCBs using Surface Mount Technology (SMT), test pads must be used since probing may damage the leads and open solder connections may be temporarily connected when the probe presses the leads onto the trace surface.

Test Probe Sizes
Test pad diameters should be between 0.015" to 0.040" nominally 0.035" when using standard 100-mil, 75-mil, or 50-mil test probes and should have an adequate solder surface to ensure reliable probe contact. 30-mil to 15mil probes are more fragile, more expensive, and less reliable. During test fixture layout, every attempt should be made to minimize the need for 30-mil to 15mil probes. For greater accessibility on fine-pitch devices, test pads should be staggered to allow 50-mil spacing.

Probing Connectors
When probing connectors, it is typical to probe the solder side of a through hole mount with a crown shaped test probe tip. Test access can be obtained through the connectors and the connectors can be tested. Special test probe tip styles are available to fit a wide variety of female connectors. Male connectors can be tested using special shrouds with cupped style probe tips up inside the shrouds.

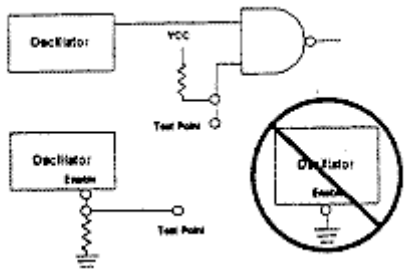
Vias
Where via probing is necessary, soldering or gold plating the vias provides a good probing surface. Vias must not be solder-masked as this will insulate and block probe contact.

Balance Probe Density, Vacuum Only
One of the great advantages of mechanical fixtures is that they do not require a balance of probe density. For vacuum fixtures only. To ensure PCB coplanarity, increase probing precision, and minimize component damage due to PCB flexing, test pad density should not exceed 12 per square inch (8 oz. probes). Excessive probe density may hinder proper sealing of vacuum fixtures. In every case, probing densities must be carefully planned to achieve the best testability.

Tall Components
Tall PCB components (> 0.35") necessitate milling the test fixture for extra clearance. As a precaution to avoid damage to the component and to prevent probe-induced shorts, test pads should not be placed within 0.1" of such components.

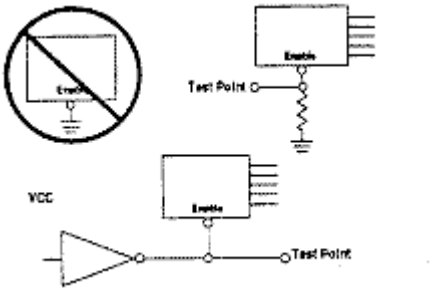
Electrical Design Considerations.
There are several fundamental design considerations that can have a major impact on a PCB's testability and, therefore, its cost.

Power Distribution
While the current handling capacity of standard probes is 1 amp, a practical limitation of 1/2 amp will guarantee more efficient probe performance and reliable power distribution. Power distribution should take place across the entire board with at least three test points for the first amp and another test point for an additional 1/2 amp. Additional test points must be included for power supply sense lines, as well as grounds and returns, especially in digital logic testing. Any PCB changes, i.e., jumpers or components on the probe surface, must be positioned carefully so as not to interfere with probe access.



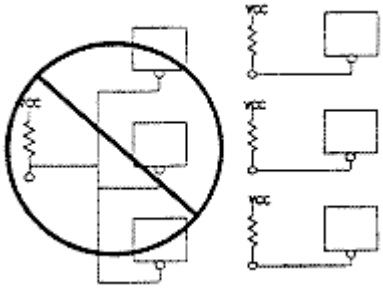
Clock Circuits

Clocks
Typically on-board clocks must be disabled to effectively test the rest of the circuit Clock sources must be controllable from the tester.



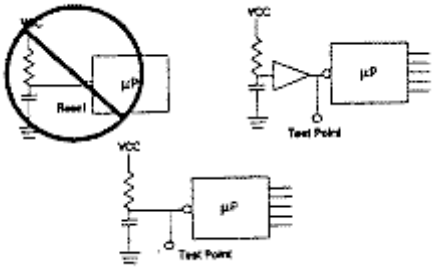
Enabling Test

Enabling Test
External control or output lines must not be tied directly to ground or to the VCC. Otherwise, it's impossible to use available test library elements easily, leading to a more complex and more costly test routine.

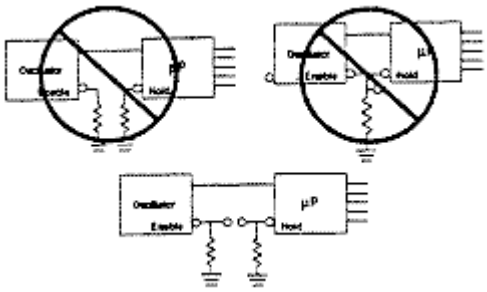


Separate Resets and Enables

Similarly, separate reset, control, and enable lines must not be tied through a common resistor as this prohibits independent testing of each device.

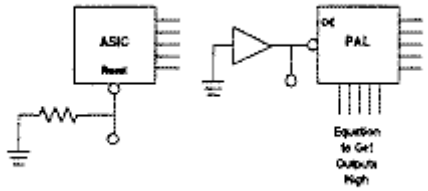


Resetting Things



Keep Resets and Enables Separate

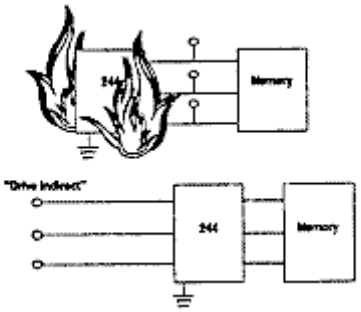
Power-on reset circuits must be able to be driven by the tester to achieve a known circuit state.



ASICs and PALs

Complex Devices
Make sure that the reset line to an ASIC or the output enable lines on a PAL are accessible to the tester. You may alternatively provide a simple equation that can be entered by the tester to set the outputs of a PAL to a known state.

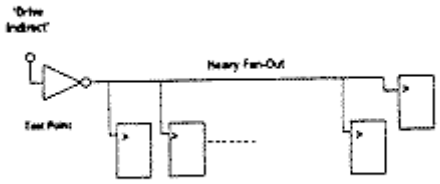
Unused Pins
All unused pins must be nailed with a test pin to ensure that faults associated with these unused pins do not propagate through the circuit.



Drive High Powered Devices by the Inputs

Drive Inputs
Many times, lengthy test backdriving of a power device, such as a 244, can lead to device destruction due

to excessive heat build-up. Driving the inputs rather than driving the outputs should be used whenever possible to avoid excessive backdrive on power devices with heavy fan-out capabilities.



Serial Chains Waste Test Time

Long Serial Chains Waste Time
Long serial chains also require special handling to prevent test times from becoming excessive. Breaking the chain with test access generally slashes the test time by orders of magnitude.

Flash
Flash EPROMS require special testability consideration. Do not program the protection bit until after the test Do not use Hardware Fault Insertion as it might re-program the device. Program first... then verify.

Battery on Board
An on-board battery requires a jumper because it is difficult to detect shorts around a battery.

Cluster Test
A bell grid array essentially has very limited access to its nodes. This often requires a form of cluster test in which an EGA is tested in conjunction with other devices that define a more testable functional block.

Mixed Signal Devices
Many analog and mixed signal devices can react adversely to the electrical loading of tester and fixture. Test points need to be buffered or placed very close to the signal source; alternatively, the device can be tested as a cluster.

It's there...but can I probe it?
Circuit nodes fall into two categories -- those that are accessible or not and those that are probeable or not. Accessible nodes might not be probeable due to tester loading on the circuit An inaccessible node might be probeable through indirect means such as Boundary Scan virtual nail. Unprobeable and inaccessible nodes are either untestable or require alternative means such as cluster test, etc.

New Test Approaches
Many innovative testing strategies are being introduced that will enhance the likelihood of testability. These include the adoption of Boundary Scan designs, automated test model development, and analog testing of digital opens.

The Testability Challenge
Regardless of the trends in system test capability, the basic challenge for test engineers is not to change the design but rather to make the designer a believer in testability.