Lecture 7

Microprocessor Architecture

- Control Path
- Data Path
- Ram (in a PC)
- Memory (instructions)
- Memory (data)
- RAM (Controller)
- Memory Protection Units
- Memory Management Units
- Programmed instruction
- Flash (in controller)
- Data

Microchip RX 62N

- Data path = 32 bits, 100 MHz
  vs. 2.6 GHz Intel
- FPU -> Floating Point Unit
- Cost - more silicon
- Memory
  - RAM 96 K Bytes
  - Flash (ROM) 512 K Bytes
  - Data Flash (non-volatile) 32 K Bytes
  - Diagnostic Data
  - Calibration Data
- Address space = $2^{32} = 4G$
ECGR 4101/5101

Lecture 7

* Clock - built in
* Reset
* DMA - Direct memory access
* Timers/Counters
* Serial Ports
* Communication
* A/D, D/A Converters

Operations: +, -, *, /

* Carry (c)
* Negative
* Positive
* Zero
* Overflow

Status word:
* Interrupt level
* Interrupt enable

Flags:

\( a = b \)

\( a - b = c \)

if zero, then equal
if not equal
Figure 3.5  Block diagram. Source: Hardware Manual, Renesas 32-Bit Microcomputer, RX Family/RX600 Series, Renesas Electronics America, Inc., 2010, Figure 1.2, page 1–12.
Figure 3.6  Register set of CPU. Source: Hardware Manual, Figure 2.1, page 2–2.
CHAPTER 3 / ORGANIZATION AND ARCHITECTURE...

1. Integer:

   | Signed byte (8-bit) Integer | b7   | b0   |
   | Unsinged byte (8-bit) Integer | b7   | b0   |
   | Signed word (16-bit) Integer | b15  | b0   |
   | Unsinged word (16-bit) Integer | b15  | b0   |
   | Signed longword (32-bit) Integer | b31  | b0   |
   | Unsinged longword (32-bit) Integer | b31  | b0   |

**Figure 3.10** Integer. Source: Hardware Manual, Figure 2.2, page 2–14.

2. Floating-Point:

   The IEEE standard defines four different types of precision for floating point operations. They are single precision, double precision, single-extended precision, and double-extended precision. Most of the floating-point hardware follows IEEE 754 standard’s single and double precision for floating point computations. RX family supports single precision floating-point computation. There are in total eight operations that can be done with such floating-point operands: FADD, FCMP, FDIV, FMUL, FSUB, FTOI, ITOF, and ROUND.

   | b31 |
   | S   |
   | E   |
   | F   |

**Figure 3.11** Floating point. Source: Hardware Manual, Figure 2.3, page 2–14.

Single-precision floating-point
S: Sign (1 bit)
E: Exponent (8 bits)
F: Mantissa (23 bits)

Value = \((-1)^S \times (1 + F \times 2^{-23}) \times 2^{E-127}\)
### Chapter 3 / Organization and Architecture

![Data arrangement in registers](source/ Hardware Manual, Figure 2.6, page 2-21)

<table>
<thead>
<tr>
<th>Data type</th>
<th>Address</th>
<th>Little endian</th>
<th>Big endian</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-bit data</td>
<td>Address L</td>
<td>b7 b6 b5 b4 b3 b2 b1 b0</td>
<td>b7 b6 b5 b4 b3 b2 b1 b0</td>
</tr>
<tr>
<td>Byte data</td>
<td>Address L</td>
<td>MSB</td>
<td>MSB</td>
</tr>
<tr>
<td>Word data</td>
<td>Address M</td>
<td>MSB</td>
<td>MSB</td>
</tr>
<tr>
<td></td>
<td>Address M+1</td>
<td></td>
<td>MSB</td>
</tr>
<tr>
<td></td>
<td>Address N</td>
<td></td>
<td>MSB</td>
</tr>
<tr>
<td></td>
<td>Address N+1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Address N+2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Address N+3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

![Data arrangement in memory](source/ Hardware Manual, Figure 2.7, page 2-21)

#### 3.2.6 Bus Specification

In total, there are five different types of buses in RX62N microcontroller board. The following section lists various bus specifications. It describes whether the bus operates in synchronization with a clock or not.

1. **CPU bus:**
   - Instruction bus:
     - It is connected to the CPU and to the on-chip memory such as on-chip RAM and on-chip ROM. It operates in synchronization with the system clock (ICLK).