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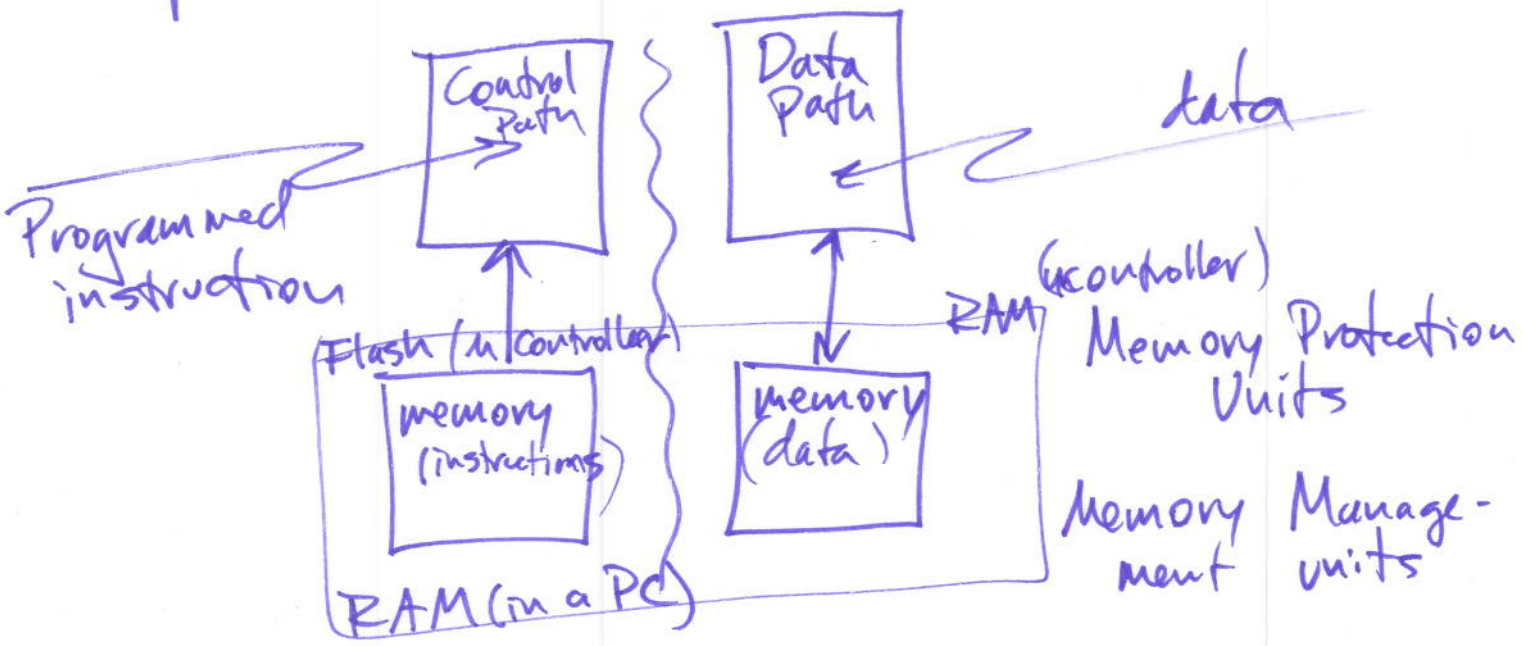
# µprocessor architecture




Renesas RX 62N →

* Data path = 32 bits, 100 MHz
  Vs 2.6 GHz Intel
* FPU → Floating Point Unit
  Cost – more silicon
* Memory
  - RAM 96K Bytes
  - Flash (ROM) 512K Bytes
  - Data Flash (non-volatile) 32K Bytes
    *Diagnostic Data
    *Calibration Data
  - Address space = $2^{32}$ = 4G

* Clocks - built in
* Reset
* DMA - Direct memory access
* Timers / counters
* Serial ports
* Communication
* A/D, D/A Converters

---

Operations +, -, *, ÷

* Carry
* negative
* positive
* zero
* overflow

→ flags

(a == b)

↑ a - b = c

if zero, then equal

if !zero, not equal

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Status word

* Interrupt level IPL
* Interrupt enable

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(3)



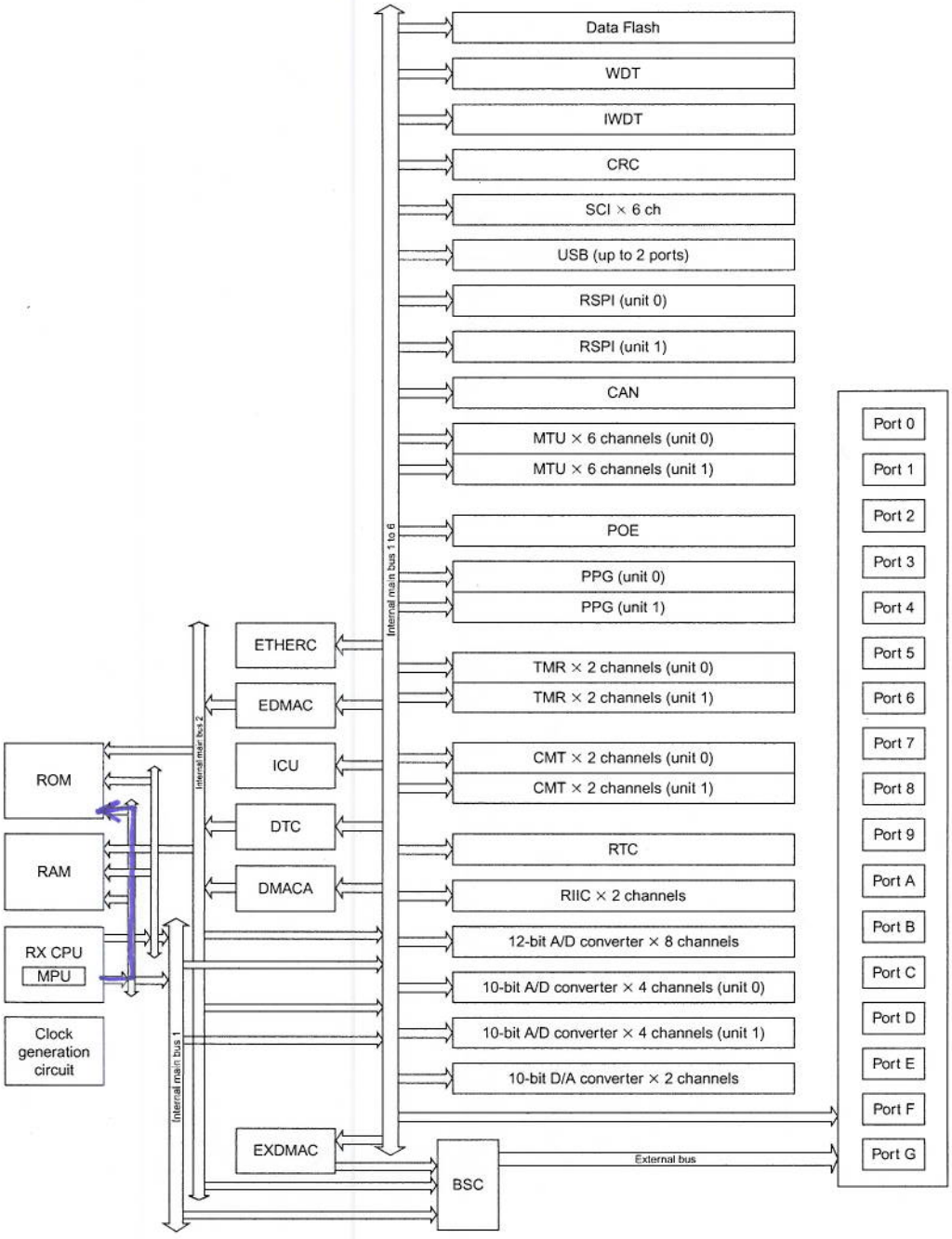


**Figure 3.5** Block diagram. Source: *Hardware Manual, Renesas 32-Bit Microcomputer, RX Family/RX600 Series,* Renesas Electronics America, Inc., 2010, Figure 1.2, page 1–12.

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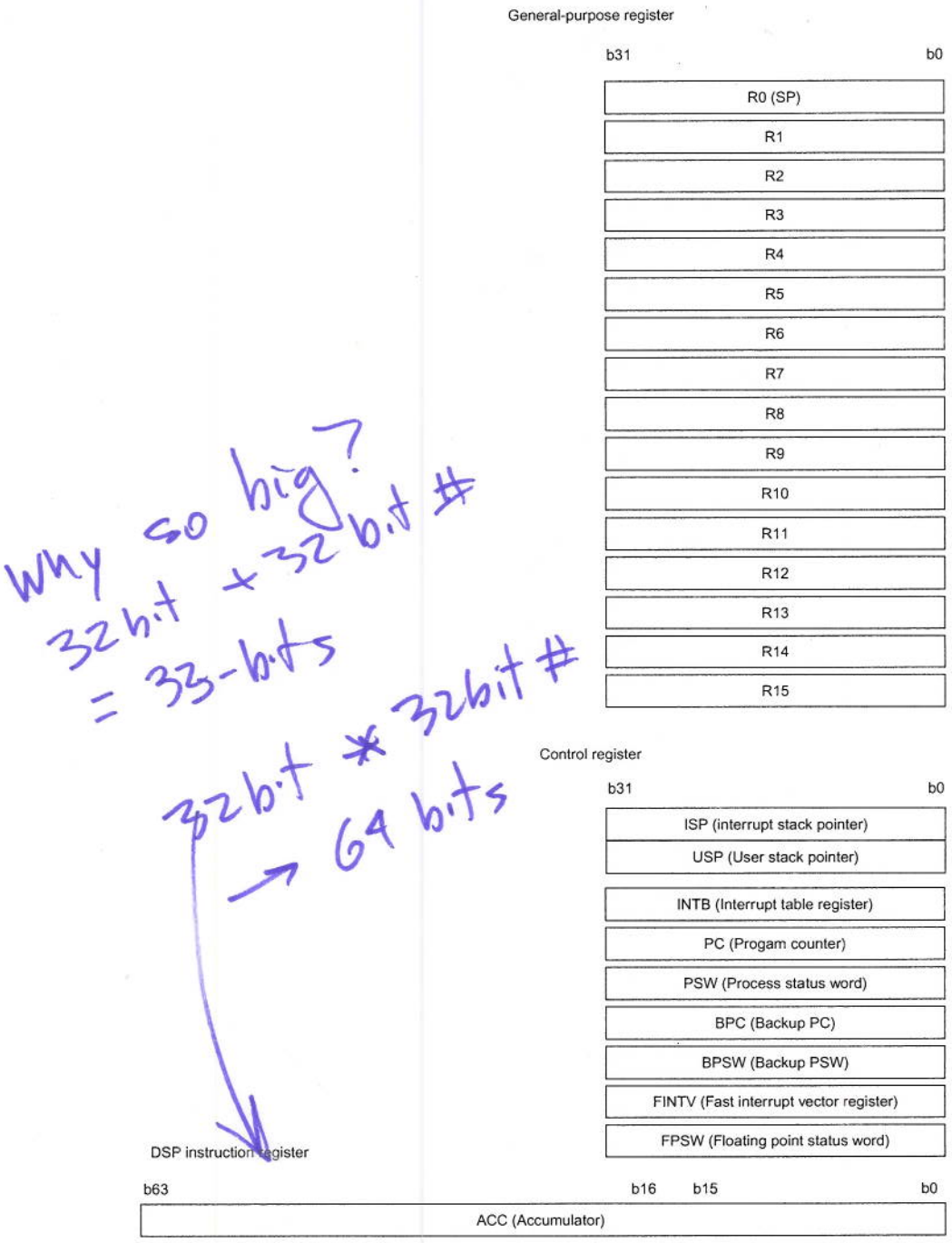


**Figure 3.6** Register set of CPU. Source: *Hardware Manual,* Figure 2.1, page 2–2.

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1. **Integer:**

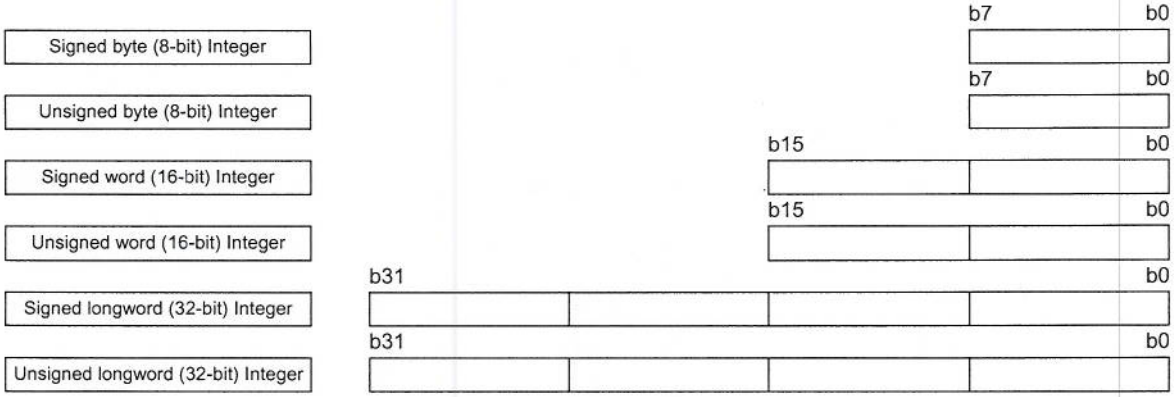


**Figure 3.10** Integer. Source: *Hardware Manual,* Figure 2.2, page 2–14.

2. **Floating-Point:**
The IEEE standard defines four different types of precision for floating point operations. They are single precision, double precision, single-extended precision, and double-extended precision. Most of the floating-point hardware follows IEEE 754 standard's single and double precision for floating point computations. RX family supports single precision floating-point computation. There are in total eight operations that can be done with such floating-point operands: FADD, FCMP, FDIV, FMUL, FSUB, FTOI, ITOF, and ROUND.

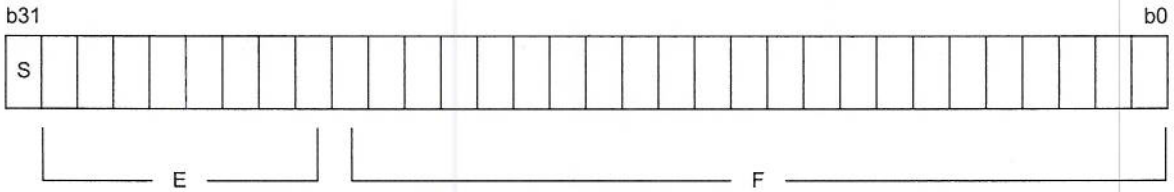


**Figure 3.11** Floating point. Source: *Hardware Manual,* Figure 2.3, page 2–14.

Single-precision floating-point
S: Sign (1 bit)
E: Exponent (8 bits)
F: Mantissa (23 bits)

$$\text{Value} = (-1)^S \times (1 + F \times 2^{-23}) \times 2^{(E-127)}$$

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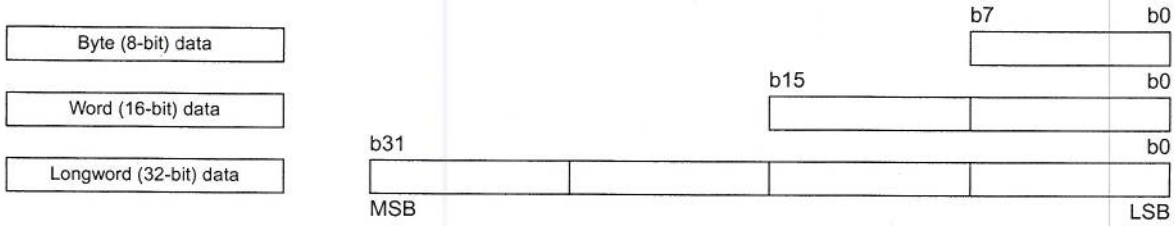


**Figure 3.15** Data arrangement in registers. Source: *Hardware Manual,* Figure 2.6, page 2–21.

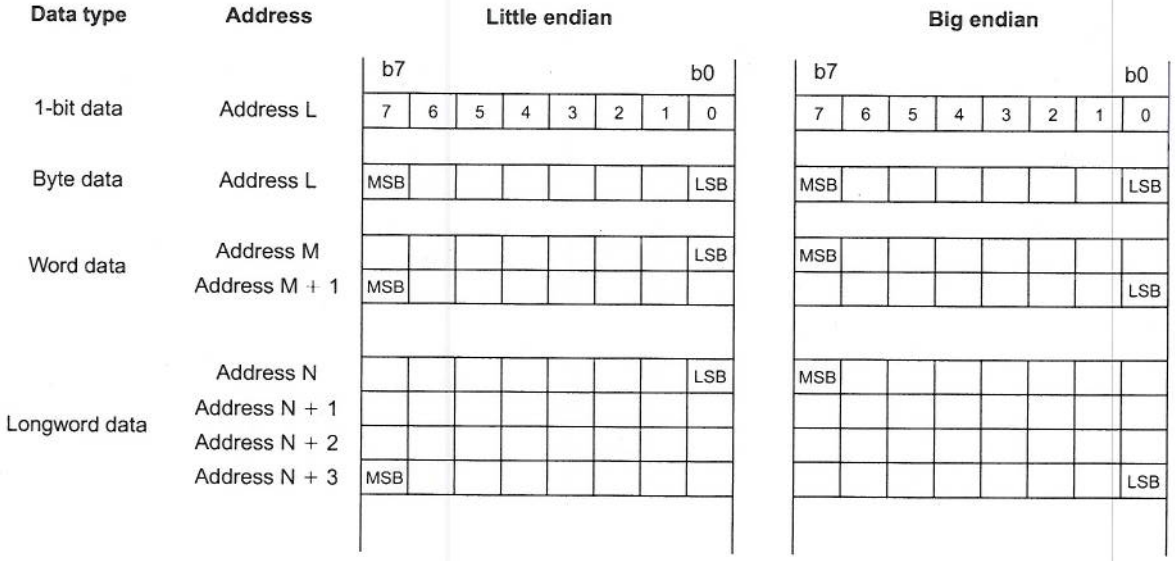


**Figure 3.16** Data arrangement in memory. Source: *Hardware Manual,* Figure 2.7, page 2–21.

### 3.2.6 Bus Specification

In total, there are five different types of buses in RX62N microcontroller board. The following section lists various bus specifications. It describes whether the bus operates in synchronization with a clock or not.

1. **CPU bus:**
   - Instruction bus:
     It is connected to the CPU and to the on-chip memory such as on-chip RAM and on-chip ROM. It operates in synchronization with the system clock (ICLK).