

# Digital Design -

ECGR 2181 Quiz 9

2015-11-03

Name: \_\_\_\_\_

Student ID: \_\_\_\_\_

①

Section: \_\_\_\_\_

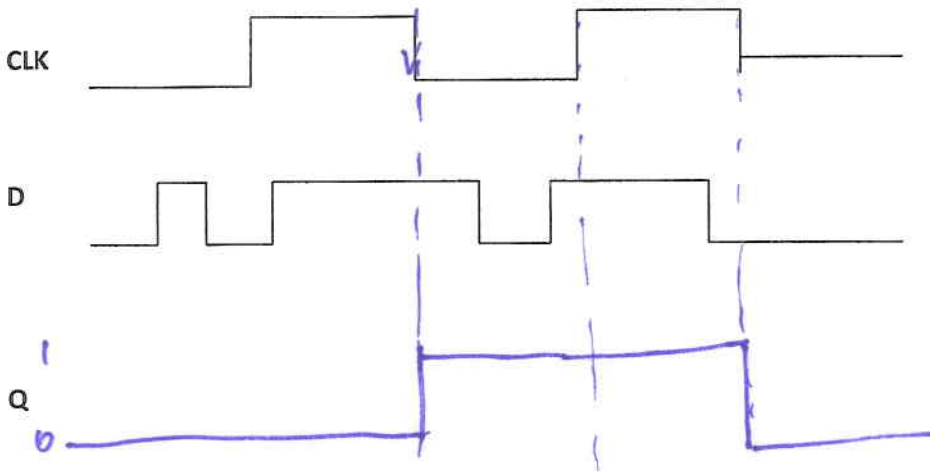
(1 point for clearly printed name)

1. What is the **TIME** and **DATE** of Exam 2? (1 point)

2. What is the difference between a Flip Flop and a Latch? (3 points)

*Example of another problem*

3. Given the following Clock (CLK) and Data Input (D), draw the D Flip-Flop (~~Rising Edge~~ *Falling Edge*) waveform output (Q) (5 points), *Q starts at 0*



Question:

②

Consider the design on page 23 of the notes. How many NOT gates, AND gates, and NOR gates are in the design?

3 registers (5 bit)  
each register has 5 D flip-flops  
each D flip flop has a NOT gate and 2 D latches  
each D latch has one NOT gate, 2 AND gates, and 2 NOR gates

	gates	latches	flip-flops	registers	
NOR =	$2 * 2$	$* 2$	$* 5$	$* 3$	$= 60$
AND =	$2 * 2$	$* 2$	$* 5$	$* 3$	$= 60$
NOT =	$(1 * 2) + 1$	$* 2$	$* 5$	$* 3$	$= 45$

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Combinational  $\rightarrow$  Valid Slide 33 (3)

Call	Cancel	Q	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Call	Cancel	Q	D
00	0	1	0
01	1	1	1
11	0	1	1
10	0	1	1

Call +  $\overline{\text{Cancel}}$  Q

