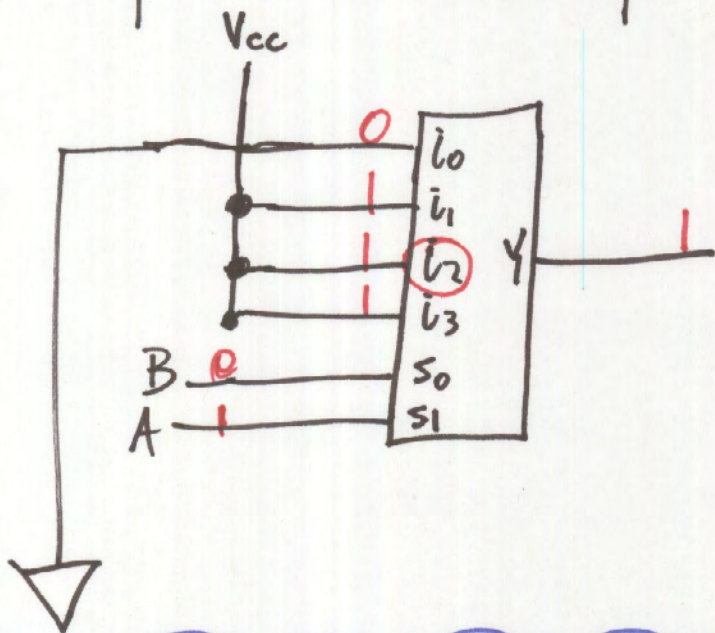


TT-OR

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

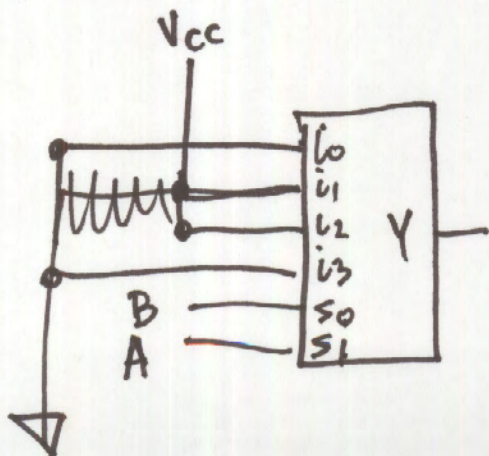
MUX

A	B	Y
0	0	$i_0 \rightarrow 0$
0	1	$i_1 \rightarrow 1$
1	0	$i_2 \rightarrow 1$
1	1	$i_3 \rightarrow 1$



This is how you make an OR gate from a MUX

Make an exclusive OR gate with a MUX



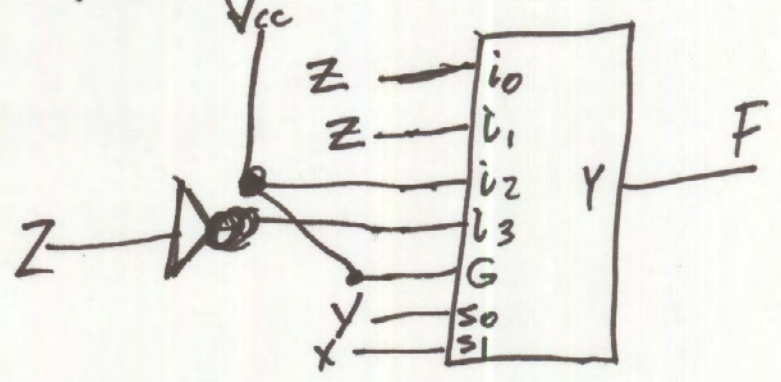
BA	$S_1 S_0$	Y
00	i_0	0
01	i_1	1
10	i_2	1
11	i_3	0

AB	Y XOR
00	0
01	1
10	1
11	0

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X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Implement using a single 4-to-1 MUX



Test question ????????

X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Implement using a single 4-to-1 MUX

