M16C/62

Using the M16C/62 CRC

1.0 Abstract

The register sets of the M16C/62 devices contain a Cyclic Redundancy Check (CRC) calculating peripheral. This gives the user the ability to quickly calculate a CRC given a stream of data.

2.0 Introduction

This article will not only explain how to use the CRC circuitry provided by the M16C, it will also explain the theory behind CRC and provide some helpful hints when developing with this error detection algorithm.

The CRC calculation circuit detects an error in data blocks. The microcomputer uses a generator polynomial of CRC_CCITT $X^{16} + X^{12} + X^5 + 1$ to generate CRC code.

The CRC code is a 16-bit code generated for a block of a given data length in multiples of 8 bits. The CRC code is set in a CRC data register each time one byte of data is transferred to a CRC input register after writing an initial value into the CRC data register. Generation of CRC code for one byte of data is completed in two machine cycles.

3.0 A Lesson in CRC and the CCITT Polynomial

In hardware, the CRC circuitry is quite easy to implement. It consists of 16 D-type flip-flop and some XOR gates. In CRC, new 8-bit values are shifted in order to manipulate the existing 16-bit value representing the current CRC result up until that point. For the CRC_CCITT polynomial, $X^{16} + X^{12} + X^5 + 1$ (or $X^{16} + X^{12} + X^5 + X^0$), the power X is raised to represents the bit location that needs to be Exclusive OR-ed with the bit that will become the overflow bit each time a new bit is shifted in.

For a refresher of the truth table for an Exclusive OR, see Table 1.

Table 1 Exclusive OR Truth Table

IN1	IN2	OUT
0	0	0
0	1	1
1	0	1
1	1	0

For a visual representation of the CRC_CCITT hardware, see Figure 1.

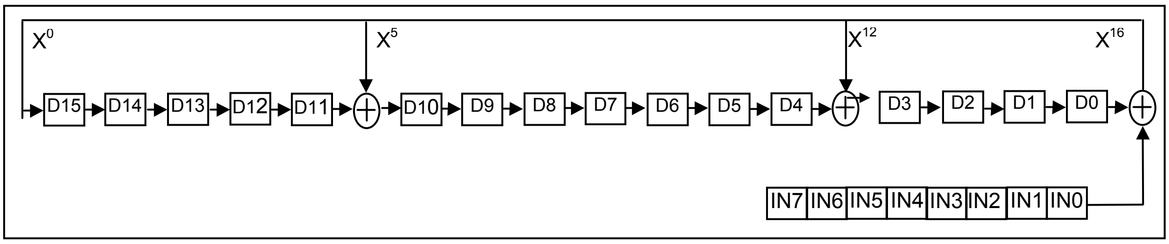

Figure 1 CRC_CCITT Hardware

Using the example in the data sheet for the M16C, the CRC data register is initialized to 0x0000 and a 0x01 is written to the CRC input register; the internal workings of the CRC_CCITT circuitry would be as shown in Table 2. The result shown in the last line would be in the CRC data register after the calculation is complete.

Table 2 CRC Data Register Example 1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X^{16}	IN
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	0
0	1	0	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0
0	0	1	0	0	0	1	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	0	0	1	1	0	0	0	1	0	0	1	x	x
1				**1**				**8**				**9**					

x = don't care

The specification then continues the example by showing a 0x23 as the next input. The result is shown in Table 3.

Table 3 CRC Data Register Example 2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X^{16}	IN
0	0	0	1	0	0	0	1	1	0	0	0	1	0	0	1	0	1
0	0	0	0	1	0	0	0	1	1	0	0	0	1	0	0	1	1
1	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0
0	1	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1	0
1	0	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0	1	0	0	1	0	1
0	0	1	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0
0	0	0	1	0	1	0	0	1	0	0	0	0	0	1	0	0	0
0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	1	X	x
0				**A**				**4**				**1**					

4.0 LSB versus MSB CRC

For our CRC hardware, values are always shifted in Least Significant Bit (LSB) first, there is no option to allow MSB first. If Most Significant Bit (MSB) first CRC_CCITT is required, reverse-bit order your data (make D0-D7 = D7-D0) before you write it to the CRC register; then reverse-bit order the resulting data.

5.0 Reference

Renesas Technology Corporation Semiconductor Home Page

http://www.renesas.com

E-mail Support

support_apl@renesas.com

Data Sheets

- M16C/62 datasheets, 62aeds.pdf

6.0 Software Code

6.1 Calculating CCITT Using the M16C CRC Registers

The M16C provides two SFR registers for CRC_CITT calculations:

- **CRC Data Register** – This is the 16-bit register that holds the current CRC result.
- **CRC Input Register** – This is the 8-bit register where data is fed to.

Therefore, the device firmware needed to represent the example above would be as follows:

```
unsigned int answer;
crcd = 0x0000;          /* Initialize data register to 0 */
crcin = 0x01;           /* add in first byte */
crcin = 0x23;           /* add in second byte */
answer = crcd;          /* answer will now equal 0x0A41 */
```

6.2 Software Algorithm for Deriving CCITT

The following is a software implementation of the CCITT polynomial. You may want to use this to create a program that will calculate the CRC_CCITT for your data so that you may incorporate the correct result into your firmware program.

```
unsigned int crc_buff = 0;    /* init our buffer to 0 */
unsigned char input = 0x01;   /* our first input will be 1 */
int i;
unsigned int x16;             /* we'll use this to hold the XOR mask */

for (i=0; i<8; i++) {
    /* XOR current D0 and next input bit to determine x16 value */
    if( (crc_buff & 0x0001) ^ (input & 0x01) )
        x16 = 0x8408;
    else
        x16 = 0x0000;

    /* shift crc buffer */
    crc_buff = crc_buff >> 1;

    /* XOR in the x16 value */
    crc_buff ^= x16;

    /* shift input for next iteration */
    input = input >> 1;
}
```

At the end of this for loop, crc_buff will equal 0x1189.

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