Logic Family Characteristics

Although ICs come in many different types with many different characteristics, the logic operations are the same. In this section, we will discuss the static and dynamic characteristics of several families of logic ICs. The most widely discussed family is TTL - Transistor-Transistor Logic. TTL is still used in many circuits and is widely used in many university laboratories because of their durability. CMOS (Complimentary Metal-Oxide Semiconductor) ICs are also very popular in many applications, especially battery operated devices, because of their low power requirements. But, CMOS ICs are easily damaged with a touch - the static discharged caused by a touch will destroy the IC.

Each family has different current, voltage, timing, and power specifications which must be observed. Many students believe the task is complete when the logic for a circuit is designed, but that is just the first step. Fanout, IC loading, and timing must also be considered.

Voltage Definitions

Figure 1 shows the definition of Noise Margins. $V_{OH}$ is the specified voltage when the output is a logic "1" (high). In TTL gates $V_{OH}$ typically has a range of 2.4 to 5v. $V_{OH}$ has a minimum specification because it is the minimum output voltage that the gate is guaranteed to output as a logic "1". The maximum $V_{OH}$ is $V_{cc}$. $V_{OL}$ is the specified voltage when the output is a logic "0" (Low). In TTL gates $V_{OL}$ typically has a range of 0 to 0.4v. $V_{OL}$ has a maximum specification because it is the maximum output voltage that the gate is guaranteed to output as a logic '0'. The minimum $V_{OL}$ is 0v.

$V_{IH}$ is the minimum input voltage allowed for the input to recognize a logic "1" (high). If the input voltage is lower, the input pin will not recognize it as a high input, and depending on its value, it may not recognize it as a low input. In TTL gates $V_{IH}$ typically has a range of 2.0 to 5v. $V_{IH}$ has a minimum specification because it is the minimum input voltage allowed for the input to recognize a logic "1". The maximum $V_{IH}$ is $V_{cc}$. $V_{IL}$ is the maximum voltage allowed for the input to recognize a logic "0" (Low). If the input voltage is higher, the input pin will not recognize it as a low input, and depending on its value, it may not recognize it as a high input. In TTL gates $V_{IL}$ typically has a range of 0 to 0.8v. $V_{IL}$ has a maximum specification because it is the maximum voltage allowed for the gate to recognize a logic "0". The minimum $V_{IL}$ is 0v.

The Noise Margin is the difference between the input and output voltages. The average Noise Margin is the average of the high and low values. This parameter is appropriately named, because it allows for "noise," such as voltage ripples, spikes, etc, to be on the line without interfering with the operation of the gate.

The High-Level Noise margin is the difference between the minimum high output voltage level and the minimum high input voltage level:

$$NM_{high} = V_{oh} - V_{ih}$$

The Low-Level Noise margin is the difference between the minimum low input voltage level and the maximum low output voltage level:

$$NM_{low} = V_{il} - V_{ol}$$

The average noise level, or simply the noise level, is the average of these two values:

$$NM = \frac{(NM_{high} + NM_{low})}{2}$$

Timing Definitions

Figure 2 shows the typical propagation delay definitions. $T_{plh}$ is the time it takes a gate to produce a high output after it recognizes the proper input stimulus and when its previous level was low. $T_{phl}$ is the time it takes a gate to produce a low output after it recognizes the proper input stimulus and when its previous level was high. Both of these specifications provide the engineer with an idea of how fast the IC will perform, and if it will perform in the circuit being developed.

Example: Image a circuit that is operating on a 100MHz clock. Can a standard TTL device work in this circuit?
Solution: A clock with a frequency of 100MHZ will have a clock period of 10ns. That means that it is possible (if the input signal changes every clock cycle) that the output will be changing at the same time the input is changing. At best, the output will always be a full cycle behind the input. At worst, with even a little deviation in parameters, the gate won't work at all.

Figure 2: Propagation Delay Definitions

Figure 3 shows the definition of rise and fall time. The rise time is the amount of time required for a signal to go from 10% of its maximum value to 90% of its maximum value. The fall time is defined as the time required for a signal to go from 90% of its maximum value to 10% of its maximum value.

Figure 2: Rise and Fall Time Definitions

Current specification are discussed in another section of this topic: "Loading and Fanout".

Family Characteristics

The following tables (Tables 1 and 2) show the voltage, current, power, and propagation delays common for several TTL family devices. Tables 3 and 4 show voltage, current, power, and propagation delays common for several CMOS devices.

Table 1 -Voltage and Current Characteristics of TTL Families

<table>
<thead>
<tr>
<th>Family</th>
<th>$V_{IH}$ min (V)</th>
<th>$V_{IH}$ max (V)</th>
<th>$V_{IL}$ min (V)</th>
<th>$V_{IL}$ max (V)</th>
<th>$I_{IL}$ max (mA)</th>
<th>$I_{IH}$ min (mA)</th>
<th>$I_{OH}$ min (mA)</th>
<th>$I_{OL}$ max (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>74xx</td>
<td>2.0</td>
<td>0.8</td>
<td>2.4</td>
<td>0.4</td>
<td>-1.6</td>
<td>.04</td>
<td>16</td>
<td>-0.4</td>
</tr>
<tr>
<td>54xx</td>
<td>2.0</td>
<td>0.8</td>
<td>2.4</td>
<td>0.4</td>
<td>-1.6</td>
<td>.04</td>
<td>16</td>
<td>-0.4</td>
</tr>
<tr>
<td>74Hxx</td>
<td>2.0</td>
<td>0.8</td>
<td>2.4</td>
<td>0.4</td>
<td>-2.0</td>
<td>.05</td>
<td>20</td>
<td>-0.5</td>
</tr>
<tr>
<td>54Lxx</td>
<td>2.0</td>
<td>0.8</td>
<td>2.4</td>
<td>0.3</td>
<td>-0.18</td>
<td>.01</td>
<td>2</td>
<td>-0.1</td>
</tr>
<tr>
<td>74Sxx</td>
<td>2.0</td>
<td>0.8</td>
<td>2.7</td>
<td>0.5</td>
<td>-2.0</td>
<td>.05</td>
<td>20</td>
<td>-1.0</td>
</tr>
<tr>
<td>74ALSxx</td>
<td>2.0</td>
<td>0.8</td>
<td>3.0</td>
<td>0.5</td>
<td>-0.5</td>
<td>.02</td>
<td>20</td>
<td>-2.0</td>
</tr>
<tr>
<td>74LSxx</td>
<td>2.0</td>
<td>0.8</td>
<td>2.7</td>
<td>0.5</td>
<td>-0.4</td>
<td>.02</td>
<td>8</td>
<td>-0.4</td>
</tr>
<tr>
<td>74ALSxx</td>
<td>2.0</td>
<td>0.8</td>
<td>3.0</td>
<td>0.4</td>
<td>-0.1</td>
<td>.02</td>
<td>8</td>
<td>-0.4</td>
</tr>
</tbody>
</table>

Table 2 -Performance Characteristics of TTL Families

<table>
<thead>
<tr>
<th>Power Dissipation</th>
<th>Standard</th>
<th>LS</th>
<th>S</th>
<th>ALS</th>
<th>AS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10mW</td>
<td>2mW</td>
<td>19mW</td>
<td>1mW</td>
<td>8.5mW</td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>10ns</td>
<td>10ns</td>
<td>3ns</td>
<td>4ns</td>
<td>1.5ns</td>
</tr>
</tbody>
</table>

Table 3 -Voltage and Current Characteristics of CMOS Families
When looking at these two tables you should notice several things. The power specs for the CMOS are quite a bit lower, as are the input currents. This is because of CMOS gate construction. We look at that below. Another item that you should notice is the difference in noise margins between CMOS and TTL. There are also a special family of CMOS devices that were specifically designed to be TTL compatible.

**Table 4 - Performance Characteristics of CMOS Families**

<table>
<thead>
<tr>
<th>Family</th>
<th>( V_{IH} ) min (V)</th>
<th>( V_{IL} ) max (V)</th>
<th>( V_{OH} ) min (V)</th>
<th>( V_{OL} ) max (V)</th>
<th>( I_{IH} ) max (mA)</th>
<th>( I_{IL} ) max (mA)</th>
<th>( I_{OH} ) min (mA)</th>
<th>( I_{OL} ) min (mA)</th>
<th>( I_{OL,TTL} ) min (mA)</th>
<th>( I_{OH,TTL} ) min (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>74HCxx</td>
<td>3.85</td>
<td>1.35</td>
<td>3.84</td>
<td>4.4</td>
<td>0.1</td>
<td>0.33</td>
<td>0.001</td>
<td>0.001</td>
<td>4.0</td>
<td>-0.02</td>
</tr>
<tr>
<td>74HCTxx</td>
<td>2.0</td>
<td>0.8</td>
<td>3.84</td>
<td>4.4</td>
<td>0.1</td>
<td>0.33</td>
<td>0.001</td>
<td>0.001</td>
<td>4.0</td>
<td>-0.02</td>
</tr>
<tr>
<td>74AHCxx</td>
<td>3.85</td>
<td>1.35</td>
<td>3.80</td>
<td>4.4</td>
<td>0.1</td>
<td>0.44</td>
<td>0.001</td>
<td>0.001</td>
<td>8.0</td>
<td>-0.05</td>
</tr>
<tr>
<td>74AHCTxx</td>
<td>2.0</td>
<td>0.8</td>
<td>3.80</td>
<td>4.4</td>
<td>0.1</td>
<td>0.44</td>
<td>0.001</td>
<td>0.001</td>
<td>8.0</td>
<td>-0.05</td>
</tr>
</tbody>
</table>

* Specification for CMOS Loads

** Specification for TTL Loads

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**Operation of TTL and CMOS Devices**

Figure 4a shows a common CMOS inverter and Figure 4b shows a common TTL inverter.

When the input to the CMOS Inverter is high, Q1 is on and Q2 is off. This will saturate Q1 (very little voltage drop) and cause the output voltage to go low. When the input is low, Q1 turns off and Q2 turns on, saturating it, and making the output voltage go high.

When the input to the TTL Inverter is high, the input current turns on the transistor, saturating it and causing the output voltage to go low. When the input is low, the transistor turns off, looking like an open circuit, and causing the output voltage to go high.

Figure 5 and 6 show the CMOS configuration for a NOR and for a NAND gate. Interesting isn’t it?
Other Characteristics

TTL: Transistor-Transistor Logic: Bipolar transistors in common-emitter configuration.
- Over 30 years old.
- Switches currents.
- Slow: 10ns/dev. typical (100 MHz).
- High power dissipation, typically 10mW/dev.
- Very reliable, commonly used.
- Power supply voltages = +5V, 0V.
- Subfamilies with different current characteristics.

ECL: Emitter Coupled Logic: Bipolar high-speed multi-emitter transistors eliminate several buffer stages.
- Switches currents.
- Fast: 1ns/dev. typical (1 GHz).
- High power dissipation, typically 40mW/dev.
- Typical power supply voltages = -8V, 0V.
- Approx 1V swing in signal from High to Low.
- Low noise margin = 0.15v

GaAs: Galium-Arsenide Logic: Bipolar high-speed transistors use a Galium-Arsenide substrate that is significantly faster than silicon.
- Switches currents.
- Very Fast: 0.1ns/dev. typical (10 GHz).
- High power dissipation, typically 200mW/dev.
- Power supply voltages = -3.5V, -5.5v, 0V.
- Approx 1V swing in signal from High to Low.
- Literally no noise margin. Requires cooling.

MOS: Metal-Oxide Semiconductor Logic: Uses a metal-oxide gate in a field-effect transistor as the switch.
- Switches voltages.
- Slow: 100ns/dev. typical (10 MHz).
- Low power dissipation, typically 1mW/dev.
- Power supply voltages = +5, -9v. Varies.
- Approx 2.5V swing in signal from High to Low.
- Large gate-to-drain capacitances limit speed.

CMOS: Complementary MOS Logic: Uses MOS-FET transistors in a complementary-biased totem pole so that one transistor is always turned off.
- Switches voltages.
- Slow: 50ns/dev. typical (20 MHz).
- Very Low power dissipation < .01mW.
- Excellent for battery-driven applications.
- Complex Power Supplies
- HC/HCT: High Speed/HS TTL Compatible: Faster than the standard CMOS: 10ns Propagation Delay (100 MHz)
- AHC/AHCT: Advanced HS/AHC TTL Compatible: Faster than the HC/HCT CMOS: 3.7 to 5ns Propagation Delay (200 MHz)