

SHRENIK MEHTA

Phone: (980)322-2212

Email: shrenik.71084@gmail.com

OBJECTIVE:

Obtain entry/mid level Embedded Software Engineer/Developer position

SUMMARY:

- Experience in designing ANSI protocols in C language, used to communicate between devices (electric meters)
- Significant experience in multi-core and reconfigurable computing on Linux platform
- Successfully developed Perl / Shell scripts on Linux/Unix platform to communicate with database
- Experience in functional verification of Microcontroller/SOC/ASIC/IC devices
- Developing windows form application using visual studio 2010 to communicate with electrical meters
- Experience working with CMMI level 3 and level 4 companies
- Experience with bug reporting tools like remedy and bugzilla and configuration management tools like CVS

TECHNICAL SKILLS:

Hardware: 8086, 8051, 8085, MIPS, RISC, Renesas M16/62C, MSP430, CY3210 PsoC, ML310, Teridian chipset

Platforms: MS-DOS, Linux, Unix, Windows 2000/XP

Languages: C, C++, C#, SystemVerilog, Vera, Verilog, VHDL, Shell, Perl, Bash, SQL, HTML, XML

Tools: Logic Analyzer, Oscilloscope, Signum emulator

Protocols: PCI Express, I2C, SPI, UART, MIPI

Software Tools: Verilog-XL, Simvision, VCS, Modelsim, Xilinx XPS, Mentor Graphics ADK, HEW, IAR, Bugzilla, Load Runner, QTP, Keil

WORK EXPERIENCE:

Austin International, York, SC

July 2009 to present

Firmware Designer

- Designed and implemented firmware for electric meters which has Teridian 8051 processor
- Implemented ANSI standard C12.18 and C12.19 protocols for electric meters
- Developing application to communicate with meter using C# on visual studio 2010
- Worked with Keil compiler and Signum Emulator for Teridian chipsets

Time Warner Cable, Charlotte, NC

March 2009 to June 2009

Engineer, System Intelligence and Monitoring

- Developed Perl scripts for Application automization
- Designed Crystal Reports for HP OpenView and Reporter Databases
- Used Loadrunner for performance testing of web based application
- Hands on experience of BAC, SiteScope, and Remedy tool

e-Infochips Limited(www.einfochips.com), Ahmedabad, Gujarat, India

Jan 2006 to July 2007

ASIC Verification Engineer

- Multiport PCI Express Networking SoC Verification: Developed and enhanced test plan and designed testcases for error signaling, debug, GPIO, implement specific sections in VERA. Also developed regression scripts in Perl
- CC2 Chip Verification: Designed stimulus generator , display monitor and refresh RAM monitor/checker modules using system-verilog and developed random, directed and corner test scenarios for Graphic Processor
- I2C Bus Protocol Verification: Developed Architecture and comprehensive test plan for I2C bus protocol and Designed I2C slave driver, monitor and scoreboard module using system verilog
- PS2 Controller Verification: Designed keyboard module for PS2 controller in VERA using RVM (Reference Verification Methodology) and integrated different device modules with the PS2 controller DUT
- 1 Bit Buffer DUT Verification: Developed verification environment and test-bench using C++

UNCC Dept. of Electrical and Computer Engineering, Charlotte, NC

Aug 2007 to Dec 2008

Teaching Assistant:

- Held recitation sessions for class section of 30 students that supplements for Electrical Engineering Design Course
- Assisted Professor with grading responsibilities

Project Work:

- **Cache Simulator:** Implemented cache simulator using C and simulated data caches suited to SPECint2006 benchmark
- **Linux Device Driver for CRC:** Designed CRC hardware core using VHDL on Xilinx's Virtex-II Pro ML310 FPGA board and build root file system with a device driver and an application to use CRC hardware
- **Autotools based Library:** Designed adjacency list and adjacency matrix graph using data structures in C language and developed an auto tools based library which performs depth first search and breadth first search for given graph.
- **Hacking the iRobot Roomba:** Designed algorithm in C language to improve the coverage area of iRobot Roomba
- **Memory Testing using March Algorithms:** Implemented a few of the March tests in C to detect stuck at faults
- **Multithreaded code of LU Decomposition:** Developed multithreaded code for LU decomposition using POSIX thread and analyzed speed up gained by parallel version over sequential version on quad-core Linux machine

EDUCATIONAL QUALIFICATION:

University of North Carolina, Charlotte at Charlotte, NC

Masters Electrical and Computer Engineering

GPA 3.9/4.0

Dec 2008

Project: Line Extraction Algorithm using Lidar for an Autonomous Robotics Vehicle

L.D. College of Engineering at Ahmedabad, Gujarat, India

Bachelors Electronics and Communication Engineering

GPA 3.8/4.0

May 2006

RELEVANT COURSES:

Embedded Systems, Advanced Embedded Systems, Computer Arithmetic, Research Tools and Techniques in Computer Engineering, Fundamentals of Reconfigurable Computing, Multicore Computing, Digital System Testing, Introduction to VHDL, VLSI System Design.