

# TI MSP430 MICROCONTROLLERS

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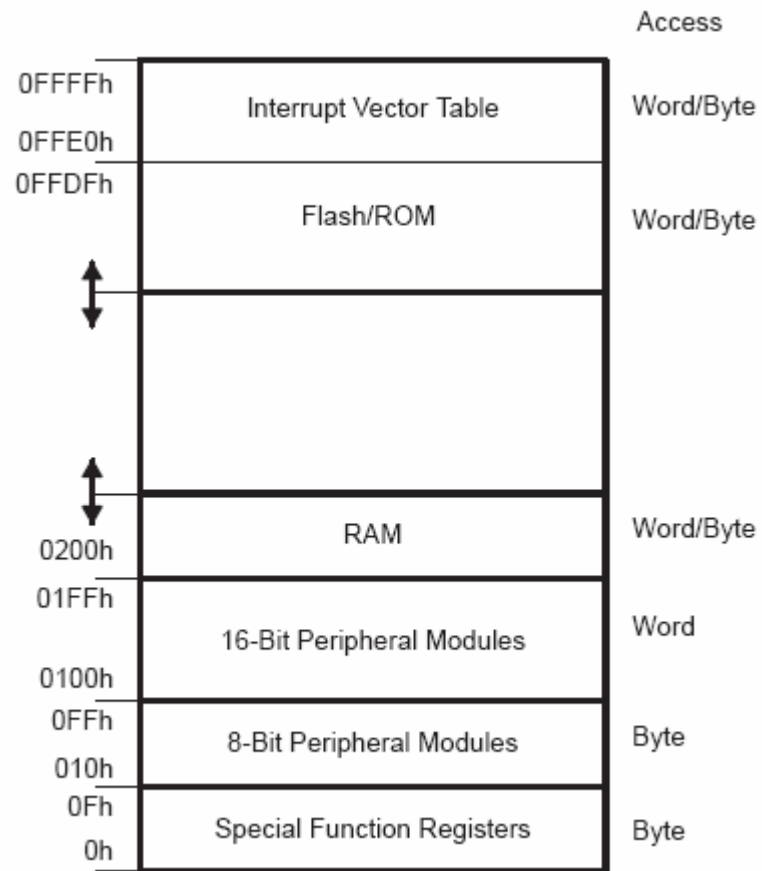
## THE MSP FAMILY

- Ultra-low power; mixed signal processors
  - Widely used in battery operated applications
  - Uses Von Neumann architecture to connect CPU, peripherals and buses
  - AVR is commonly used debugger
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## The MSP family (cont.)

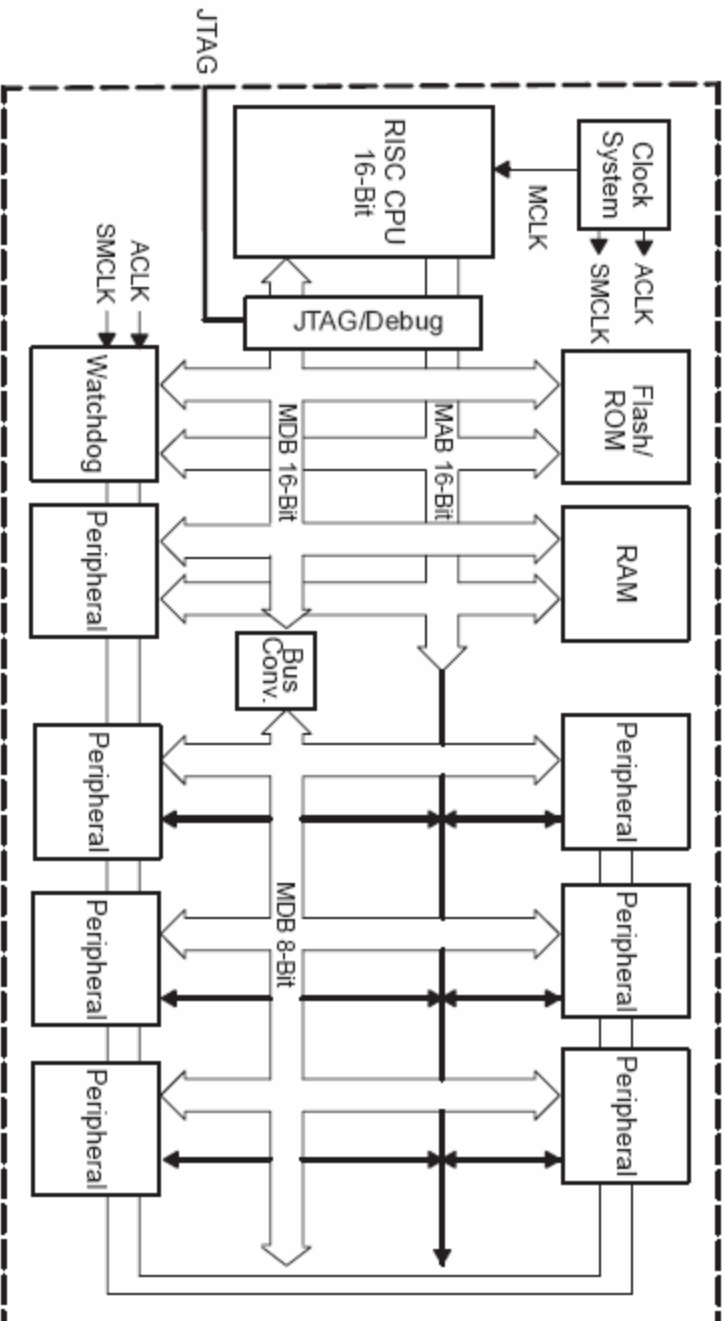
- 1 to 60 kB flash
  - 256B to 2kB RAM
  - With or without Hardware multipliers, UART and ADC
  - SMD package with 20 to 100 pins
  - MSP 430 family has 4 kB flash, 256B RAM, 2 timers and S0-20 package
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# Memory Organization



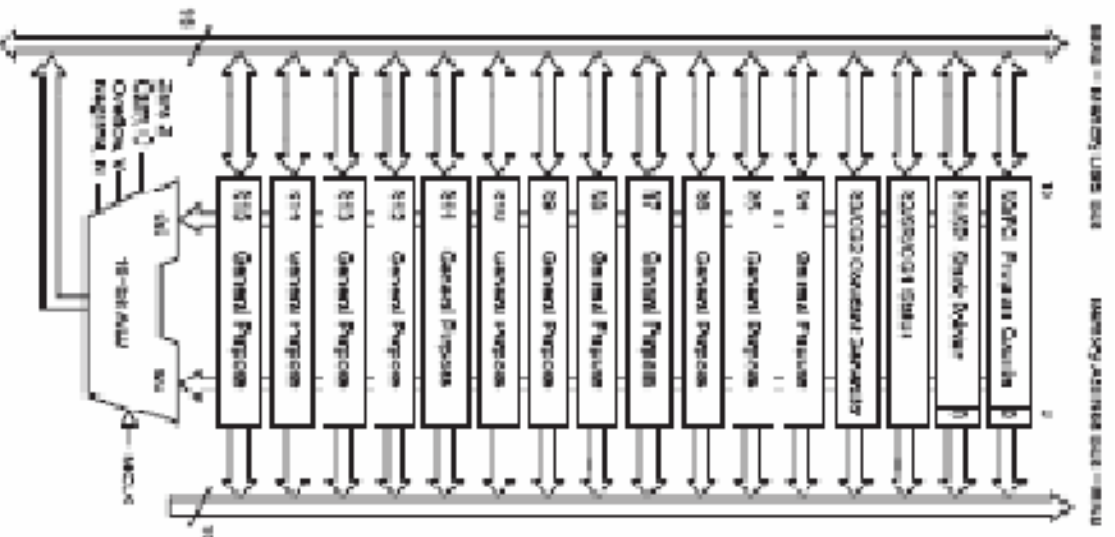
## Architecture: Basic Elements

- 16 bit RISC processor
  - Programmable 10/12 bit ADC
  - 12 bit Dual DAC for accurate analog voltage representation
  - Supply voltage supervisor for detection of Gray level
  - Programmable timers, Main and Auxiliary crystal circuits
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## CPU features

- Reduced Instruction Set Computer Architecture
  - 27 instructions wide instruction set
  - 7 orthogonal addressing modes
  - Memory to Memory data transfer
  - Separate 16 bit Address and Data buses
  - 2 constant number generators to optimize code
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## Instruction Set

- 27 “CORE” instruction and 24 “EMULATED” instructions
  - No code or performance penalties for Emulated instructions
  - Instructions can be for word or byte operands (.W / .B)
  - Classified into 3 groups
    - Single Operand Instructions: RR, RRC, PUSH, CALL
    - Dual Operand Instructions: MOV, ADD, SUB
    - Jumps: JEQ, JZ, JMP
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## Clock sub-system

Basic Clock module includes:

- LFXT1 – LF/HF crystal circuit, that uses either 32,768 Hz crystal (LF); or standard resonators in 450K-8MHz range
  - XT2 – optional HF oscillator that can be used with standard crystals or external resonators in 450K -8MHz.
  - DCO – Digitally Controlled Oscillator. Software programmable, RC characteristics
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## Clock Sub-system (cont.)

- 3 clocks for the balance of power consumption and performance
    - ACLK: uses the LFXT1 (32,7Hz)clock divided by 1,2,4 or 8 for individual peripherals
    - MCLK: uses LXT1, XT2 or DCO sources as software programmed  
Used by the CPU and system
    - SMCLK: uses LXT1, XT2 or DCO sources as software programmed for the peripherals
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## Flash Memory Organization

- Bit, Byte or Word addressable memory
  - Information memory divided into segments of 128 bytes
  - System memory has 2 or more 512 byte segments.
  - Segment is further divided into 64 bytes blocks
  - Can have segment erase and mass erase
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## Supply Voltage Supervisor (SVS)

- Used to monitor the AVcc level
  - 14 selectable ranges
  - Software accessible
  - Generates a POR interrupt
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## ADC

- Selectable 10 or 12 bit precision
  - Uses Dual Slope ADC technique
  - Monolithic 10/12 bit conversion with no missing codes
  - Higher than 200 ksps conversion rates
  - Sample and Hold
  - 8 individually configurable channels
  - Initialization by software or timer A.
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## DAC

- 12 bit DAC with selectable 8/12 bit precision
  - Straight or 2's compliment binary
  - Self calibration option for offset
  - Programmable settling time for power consumption
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## Typical Applications

- Filters – FIR, wave filtering
  - Benchmarking circuits
  - Data Encryption and Decryption
  - Flash monitor
  - Low power sensing applications
  - Random Number generation
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## Stiquitto

- Small, simple hexapod robot
- Used as research platform to study computational sensing, gait controllers, machine vision, emergent behavior etc.



## Comparison with Renesas

### **Renesas**

- General purpose uC
- 32 kB RAM, 384 kB flash
- 8 bit Data Bus; 20 bit Address bus
- 8/10 bit ADC
- 2 8 bit DAC

### **MSP 430**

- Ultra low power, signal processor
  - 256 B RAM, 4kB flash
  - 16 bit Data/ Address buses
  - 10/12 bit ADC
  - 12 bit DAC
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## References

- <http://msp430.techcontent.net/whymsp.htm>
  - [http://en.wikipedia.org/wiki/TI\\_MSP430](http://en.wikipedia.org/wiki/TI_MSP430)
  - <http://focus.ti.com/lit/ug/slau049f/slau049f.pdf>
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