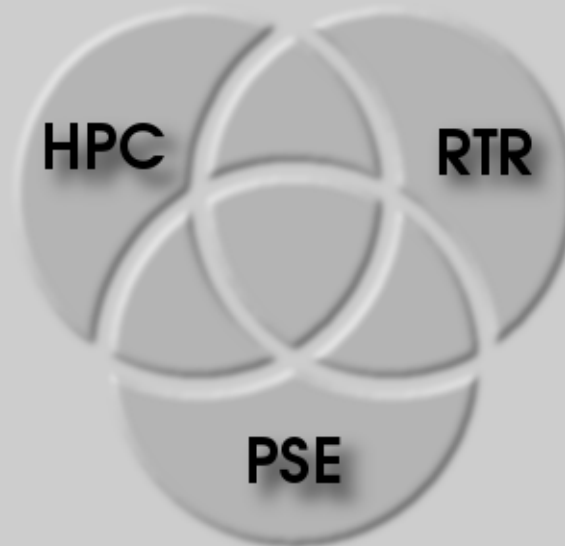


RESEARCH SUMMARY & GOALS

Ron Sass



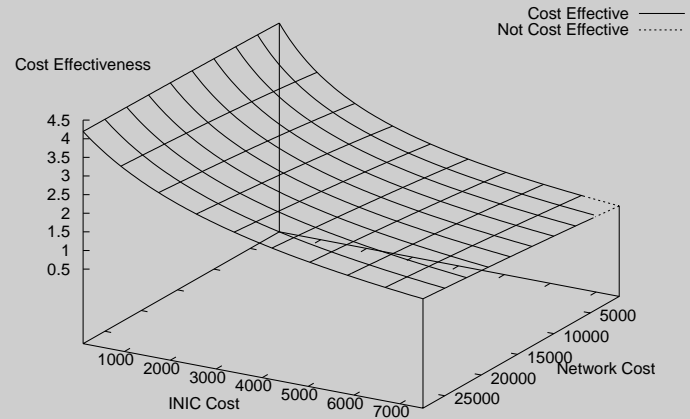
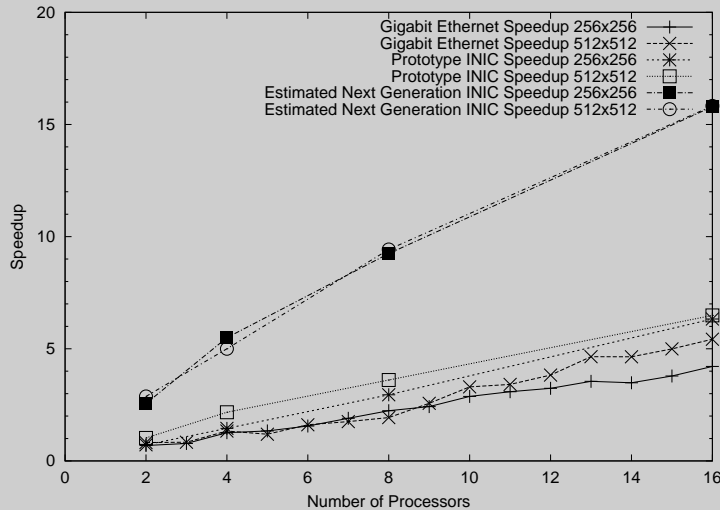
Prior/Active Sponsored Research Projects

- Reconfigurable Computing Cluster (NSF, \$167) [PI]
- Automatic Synthesis of Hardware Features (IBM, \$20K) [PI]
- Dynamic Hardware Reconfiguration to Accelerate Java-Based Embedded Systems (NSF, \$240K) [PI]
- Alternative Computing Roadmap (NASA, \$153K) [PI]
- Adaptable Computing Cluster (NSF, \$168K) [PI]
- An Operational Parallel File System for Beowulf (NASA, \$212K) [Co-PI]
- An Application Development Framework for Reconfigurable Computing (NASA, \$300K) [Co-PI]

Adaptable Computing Cluster

- basic idea: put user-programmable FPGA in the network interface of a commodity (Beowulf-class) cluster
- contribution: showed that simple operations on data *as it travels through the network* can have much larger effect on performance of the system

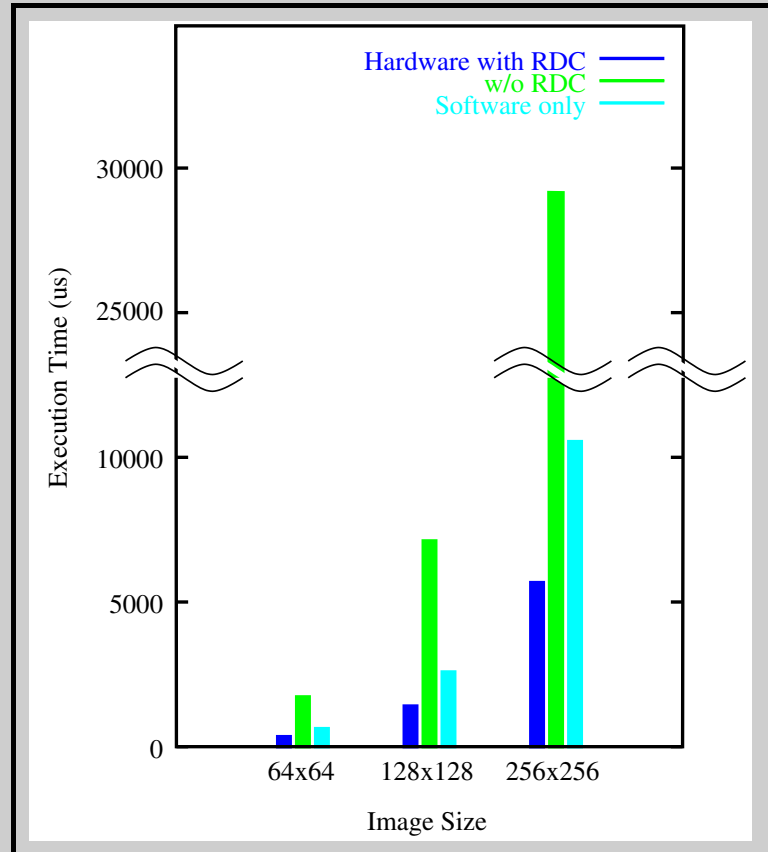
Adaptable Computing Cluster (cont'd)



Reconfigurable Data Cache

- basic idea: use data dependence information from compiler to build application-specific cache
- contribution: an algorithm to determine and synthesize design of maximum performance based on resources and bandwidth

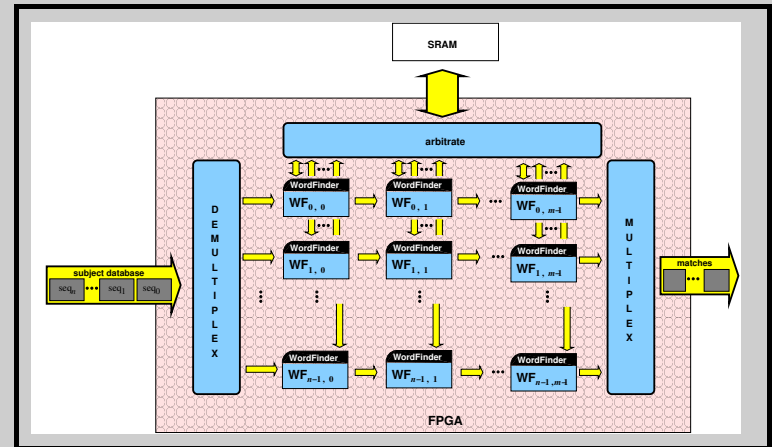
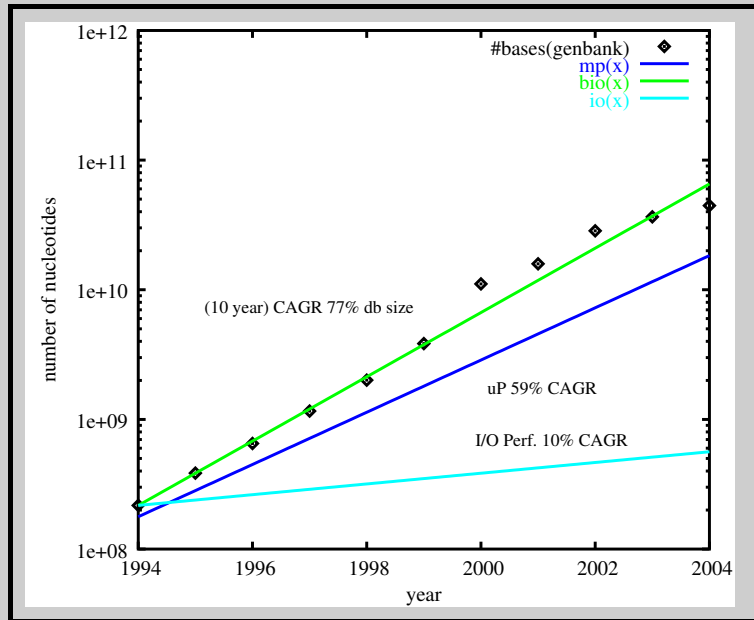
Reconfigurable Data Cache (cont'd)



RC-BLAST

- basic idea: map compute-intensive part of BLAST app to FPGA
- contribution: show that it is more cost-effective to use FPGAs than simply buying cluster of PCs

RC-BLAST (cont'd)



RCADE

- basic idea: problem-solving environment to make RC accessible to computational scientists
- contribution: a framework for building problem-solving environments

RCADE (cont'd)

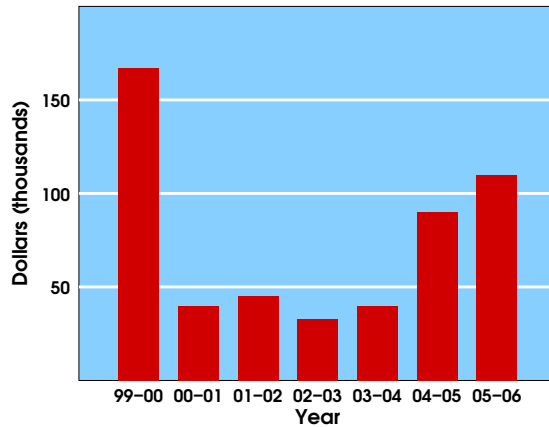
The screenshot displays the RCADE software interface, which is used for hardware simulation. The main window is titled "Editor - parl.pse.rcade.Editor" and shows a circuit schematic with components like "mux", "mul1", "mul2", and "sub1". A smaller window titled "multexam" shows a detailed schematic of a multiplier circuit, including components like "FEFP", "Multiplier-1", "Subtractor", and "Multiplier".

On the right side, there is a "DynamicTestBench" window showing simulation settings and a table of wire/port values. The table is as follows:

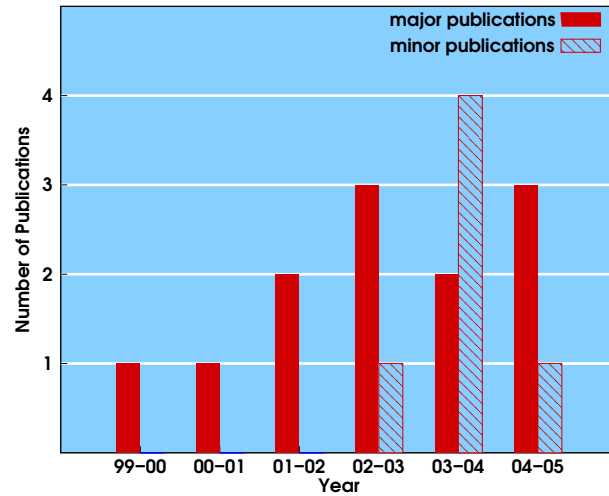
Wire/Port Name	Width	Type	Value
rst	1	IN PORT	0
in0	8	IN PORT	00
ef0	1	IN PORT	0
rd0	1	OUT PORT	0
in1	8	IN PORT	00
ef1	1	IN PORT	0
rd1	1	OUT PORT	0
in2	8	IN PORT	00
ef2	1	IN PORT	0
rd2	1	OUT PORT	0
in3	8	IN PORT	00
ef3	1	IN PORT	0
rd3	1	OUT PORT	0
out0	32	OUT PORT	00000000
outff0	1	IN PORT	0
outw0	1	OUT PORT	0

Near-Term Goals

Annual Research Expenditures



Annual Publications



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