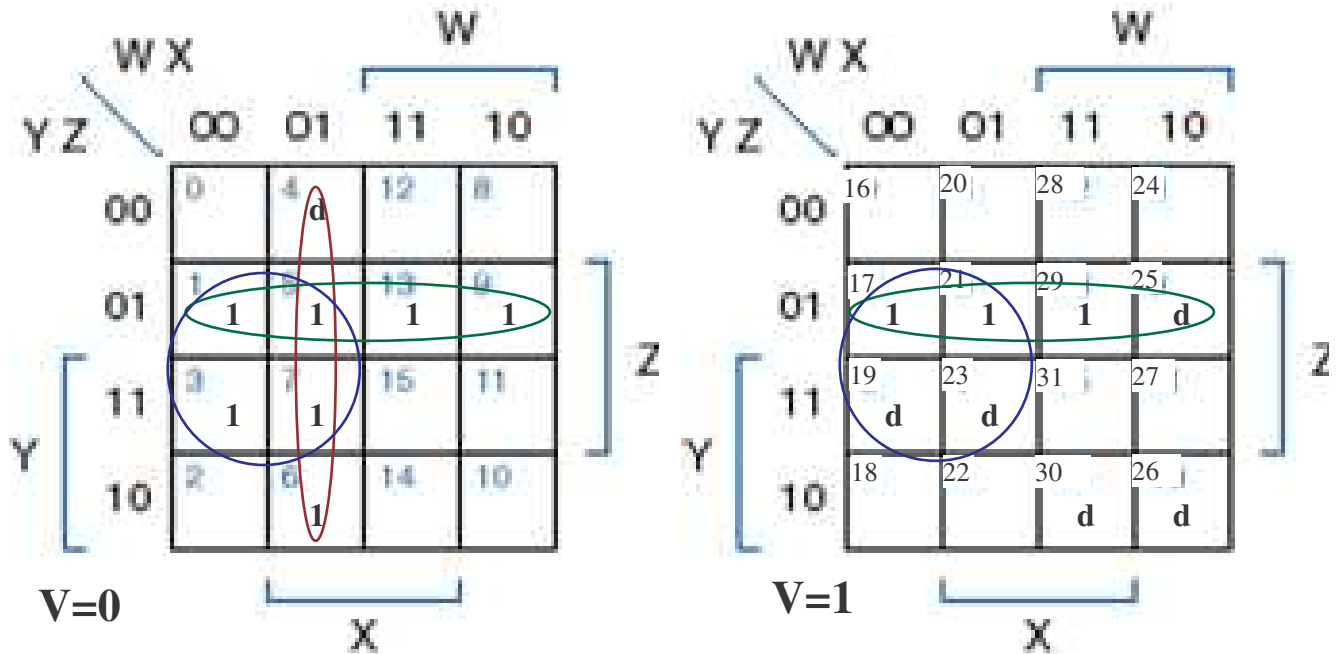


## UNC Charlotte – Spring 2006 - Exam 2 – March 30, 2005 - SOLUTION

Question	1	2	3	4	Total
Score	/30	/30	/50	/40	/150

1.  $0x04EA \div 0xFFCE = -1 * 0x04EA \div 0x0032 = -1 * 0x0019 = 0xFFE7$ , Rem 8  
 $0x03EA \div 0xFFCE = -1 * 0x03EA \div 0x0032 = -1 * 0x0014 = 0xFFEC$ , Rem 2

2.  $F = Y'Z + W'Z + V'W'X$  (note this is minimal, the d's in 26, 30 are not needed)



3. (similar to p. 280, Table 5-43)

```
library IEEE;
use IEEE.std_logic_1164.all;

entity fewgates is port
  (V, W, X, Y, Z: in std_logic;
   F: out std_logic );
end fewgates;

Architecture behavioral of fewgates is
begin
  process (V, W, X, Y, Z) begin

    F <= ((NOT Y) AND Z) OR ((NOT W) AND Z)
          OR ((NOT V) AND (NOT W) AND X);

  end process;
end behavioral;
```

4. (similar to p.317, table 5-80)

```
module fewgates (V, W, X, Y, Z, F);
  input V, W, X, Y, Z;
  output F;
  reg F;

  always @ (V, W, X, Y, Z)
    F = (~Y & Z) | (~W & Z) | (~V & ~W & X);
endmodule
```