1) (30 points) You are given two 16-bit two’s complement numbers: 0xFFCE and 0x03EA. Perform the operation 0x03EA divided by 0xFFCE. Show the quotient and remainder as two 16-bit two’s complement numbers (remainder will be positive). Show **ALL** of your work.

2) (30 pts.) Combinational Circuit Minimization: Draw a correctly labeled Karnaugh map, fill it in, and find a minimal sum of products expression for the function:

\[ F = \Sigma W,X,Y,Z(1,3,5,6,7,9,13) + d(4) \]

3) (40 pts.) Consider a simple 3-to-8 decoder with one enable (EN), three inputs (I2 to I0), and eight outputs (Y7_L to Y0_L).
   a) An input on I2 I1 I0=010 and EN=1 will produce an output of
      \[ Y7_L Y6_L Y5_L Y4_L Y3_L Y2_L Y1_L Y0_L = 00000100. \]
   a) An input on I2 I1 I0=100 and EN=1 will produce an output of
      \[ Y7_L Y6_L Y5_L Y4_L Y3_L Y2_L Y1_L Y0_L = 00010000. \]
   c) If EN=0, \[ Y7_L Y6_L Y5_L Y4_L Y3_L Y2_L Y1_L Y0_L = 00000000. \]
   Write the structural (gate-level) VHDL code to implement this device. Use the sheet provided.

4) (50 pts.) Consider a simple 8-to-3 encoder with one input enable (EI), eight inputs (I7 to I0), one output enable (EO) and three outputs (Y2 to Y0).
   a) An input of I7 I6 I5 I4 I3 I2 I1 I0 = 00001000 and EI=1 will produce an output of \[ Y2 Y1 Y3 = 011 \] and \[ EO = 1. \]
   b) An input of I7 I6 I5 I4 I3 I2 I1 I0 = 10000100 and EI=1 will produce an output of \[ Y2 Y1 Y3 = 111 \] and \[ EO = 1. \]
   c) If EI=0, \[ Y2 Y1 Y3 = 000 \] and \[ EO = 0. \]
   Draw the logic diagram of this circuit.
library IEEE;
use IEEE.std_logic_1164.all;

entity V3to8dec is
  port (}

end V3to8dec;

architecture V3to8dec_s of V3to8dec_s is

begin

end V3to8dec;