Design Review for Stiquito PCB

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Purpose of Design Reviews

1. Inspect the schematic and ensure the correct functionality is present in the design.
2. Inspect the schematic and ensure the components are of correct values and type.
3. Inspect the routing to see if there are any connection / crosstalk / or other problems.
Responsibilities

1 Designer Responsibilities
   - Display near completed design or progress of design.
   - Justify design choices and assumptions.
   - Demonstrate that the design meets project goals.
   - Make note of design problems and be prepared to fix them.

1 Reviewer Responsibilities
   - Check the design for mistakes the could cause quality and functional problems.
   - Reconsider the designers assumptions. Are they valid or need to be corrected.
   - Request the forgotten features be added.
   - Request that extra features be justified or remove to reduce cost.
Design Requirements - Schematic

1. Current Stiquito design needed correction and features added to the schematic.
   - Add JTAG interface.
   - JTAG power option selected with jumpers using 2-pin, 0.1” header on PCB.
   - Add Prototype Area.
   - Route extra I/O to the Prototype Area.
   - Correction added for A/D conversion.
   - Speed control input wired for different options.

2. Thru-hole area added for crystal to test another clock mode of the microcontroller.
3. Add decoupling to IC’s to reduce voltage sag on power rails.
4. Schematic Symbols corrected to reflect true wiring and pin outs.
5. Microcontroller I/O reordered to include new features.
6. Make everything as cheap as possible. Remove expensive parts like connectors and switches.
Values of R5 and C4 did not matter for now just needed place holder and footprints for layout.

Three modes were designed for the input P2.3.
- Mode 1: Push button speed control.
- Mode 2: Speed control pot
- Mode 3. P2.3 is a free I/O routed to prototype area.

Headers used to represent prototype area.
Crystal added to pin 5 and 6 of Micro-controller to add footprint for testing external clock mode.
Symbol for the Leg Assembly is just a “black box” representation.
Micro-controller and JTAG
Sink Driver and Leg Assembly
Design Requirements - Layout

1. Board Info
   - 2-layer with solder mask and one side population.
   - Silk Screen maybe possible but label in metal.
   - All holes plated.
   - Size: approx. 1 x 3 inches (smaller if possible)
   - 2 IC’s (Microcontroller and Sink Driver), 3 LED’s, 1 Trim Pot

2. Current Stiquito PCB have problems affecting quality and also needed the features added to the schematic.
   - Footprint for Stiquito Leg Assembly needed better fit and better pads.
   - Limit to 3 drills.
   - R and C are 0402 size. Other parts need the footprint checked.
   - Heavy traces need to ULN2803 Sink Driver and to Spine Connection of the Leg Assembly.
   - Power soldered in without connector.
Design Assumptions – Layout - 1

Leg Assembly Footprint
- Uses bolt size and nut size #0-80.
- Bolt tread dia. is 60 mils
- Nut outer dia. is 156 mils
- Padstack made with 160 mils pad and 75 mils hole this accounts for 5 mil plating. Final hole size 65 mils. May be a tight fit.
- Checked some on-line info. (expressPCB) Starting with ½ oz. copper and plating to 1 ¼ oz. the plating is ~1.7 mils thick. This gives a finished hole approximately 71.6 mils.

Leg Assembly Pad Spacing
- 3 x 2 array with 1031.25 mils spacing in the x direction and 250 mils in the y direction. The rows are offset by 31.25 mils.
- Connections for the VCC Spine and two 2nd degree of freedom pads included with footprint for ease of later placement.
- Used Cadence Layout’s Pad Array Generator to create footprint once spacing was calculated.
- Footprint could not automatically be placed using netlist. Instead a 9-pin header was place by the program then replaced later.
Main current consumption is in the nitinol wires and sink driver.
- Assumed that with 2 way gait that the current would pulse up to 0.5 amps.
- Routed power to Vcc spine connection of leg assembly at 30 mils.
- Routed power and ground to sink driver at 25 mils.
- Continued to rout power and ground at 25 mils where possible but used and minimum of 15 mils.
- Signal trace minimum 8 mils.

Trace current chart from expressPCB. 1 ¼ oz. copper.

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Layout View showing top, bottom, outline and silk screen layer.
Top and bottom layer displayed individually.
Supporting Documentation

1. MSP430F1101A Data Sheet
2. ULN2803/04 Data Sheet (Toshiba)
4. Data Sheets for components with footprint information.
5. MSP430-H1121-B Header Board Data Sheet for information on the JTAG interface